

# Historical Canberra MCAs

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Reference Manual

9234340A

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The information in this manual describes the product as accurately as possible, but is subject to change without notice.

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# 1. Introduction

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This publication contains instructions for the System 100 and AccuSpec MCAs. For newer MCAs, the instructions are included in each MCA's manual.

Chapter 2, Setting up a MCA Input Definition:

- Using the MID Wizard, on page 2.
- Using the MID Editor, on page .
- Setting up an AccuSpec MCA, on page 12.
- Setting up a System 100 MCA, on page 22.

Chapter 3, Hardware Installation, and Chapter 4, Technical Information, cover technical information about the System 100 and AccuSpec MCAs.

## 2. Historical MCA Input Definitions

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The first step in using your Genie-2000 system is to let it know the number and types of MCAs that are installed in or connected to your system, by way of an MCA Input Definition (MID).

### **MID Wizard or MID Editor**

For most systems, you'll want to use the MID Wizard to help you set up your MCA's Input Definition quickly and easily.

If your Input Definition is more complex than the MID Wizard was designed to handle, you'll have to use the MID Editor to create your definition. It is covered in detail starting on page 6.

## The MID Wizard

### **Restrictions**

The Wizard does not support:

- Definition of multiplexer (MXR) inputs. This includes devices such as the Alpha Analyst.
- Configuration of remote VDMs.
- Definition of two-ADC inputs from a single AIM device.

For these situations, you must use the MID Editor (page 6).

### **Using the Wizard**

To use the MID Wizard, open the Genie 2000 folder and select the MID Wizard icon to see the Step 1 screen.

Note: The screens shown here are examples for this tutorial; the screens you see may vary, depending on the MCA type you specified.

#### **Step 1**

The first screen (Figure 1) lets you select the MCA you're creating the definition for.

Click on the '+' next to the "Network MCAs" board type, choose DSA-2000, then click the Next button.

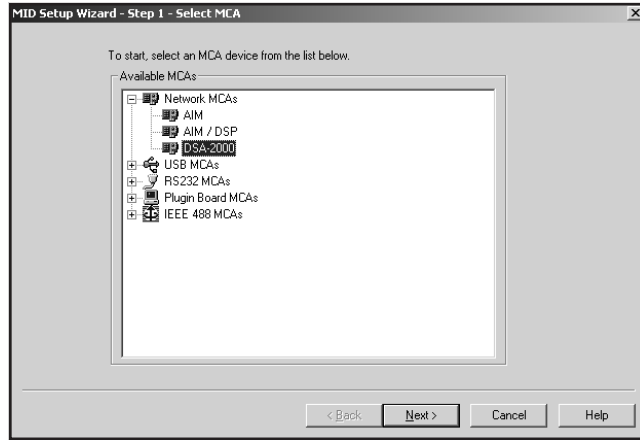


Figure 1 Step 1

## Step 2

The Step 2 screen (Figure 2) will ask you to define the MCA's Full Memory size, Station address, and whether the DSA-2000's input is to be PHA mode or MCS mode.

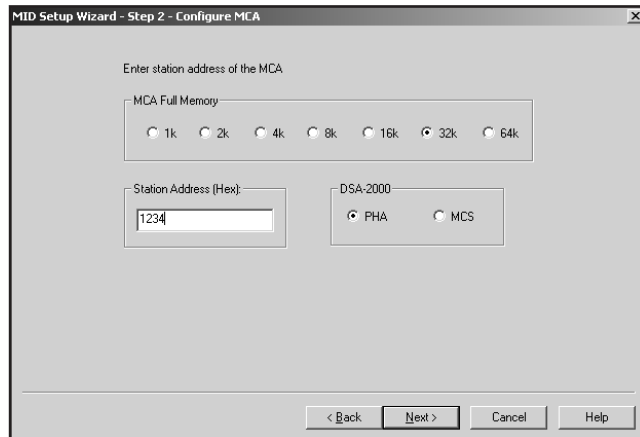


Figure 2 Step 2



### Step 3

The Step 3 screen (Figure 3) asks for an Input Name, the Detector Type, Memory Groups and the Number of Channels.

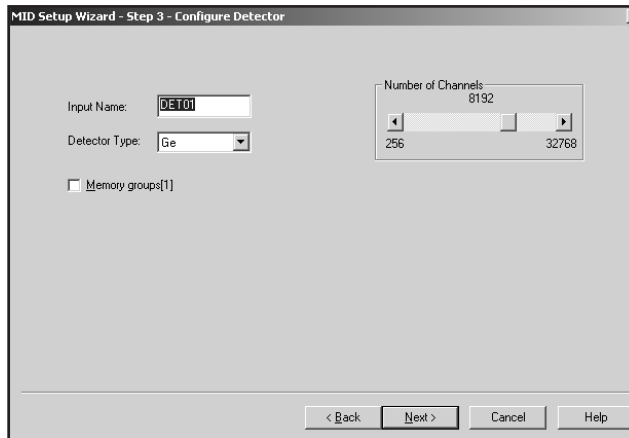


Figure 3 Step 3

You can change the default Input Name if you like, but if the field is empty, you won't be able to go to the next screen

With the Memory Groups box selected, the full memory can be divided into two or more memory groups. The number of groups depends on the the Number of Channels slider's setting.

### Steps 4 and 5

Steps 4 and 5 are not used in setting up the DSA-2000.

### Step 6

The Step 6 screen in Figure 4 asks you to define the high voltage power supply's Range, Voltage Limit and working Voltage.

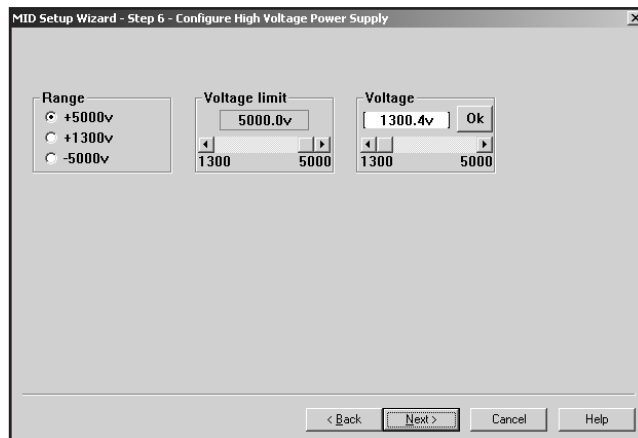


Figure 4 Step 6

### Step 7

The Step 7 screen in Figure 5 displays a summary of the current MCA's configuration for review and lets you enter the name of the MID file that the configuration is to be saved to.

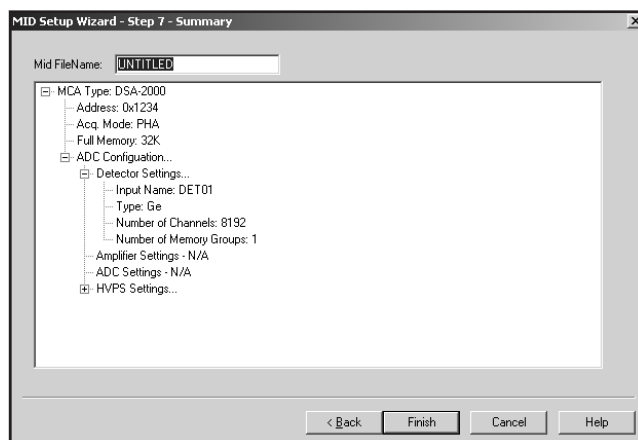


Figure 5 Step 7

### Ending the Definition

To complete your Input Definition, select **Finish**. The input that you just defined will be stored as an MID file, using the name you specified in Step 7. The new MID file will automatically be loaded into the MCA Runtime Configuration Database (described on page ).

When you select **Finish**, you will be asked if you would like to define another input. Answering No will close the Wizard.

If you didn't enter a MID filename, you won't be allowed to exit this screen. If the name you entered is the same as that of an existing MID file, the system will tell you so and go back to Step 7 to let you enter another name.

## The MCA Input Definition Editor

In addition to using the MID Editor to create a new input definition (MID File), it's used to edit an existing MID File. For instance, you might want to:

- Change the default settings for any of your MCA's programmable components
- Replace a manual HVPS with a programmable HVPS and select its default settings.

In addition, the definition of an MCA also includes things like the data acquisition mode (PHA+, PHA-, MCS, and so forth) and memory size. In short, the definition includes everything about the hardware that the software needs to know in order to use it to acquire data.

A point worth noting is that an MCA does not have to be physically installed at the time that you define it in the MCA Input Definition Editor. For example, you can define an MCA that is installed on another node of the network as "yours" even though that node happens to be off line when you set up the definition. (Of course, before you can actually use that MCA, the node must be brought on line.)

### Multiple MCA Configurations

Since MCA definitions are saved in disk files, you can have as many different definitions as you want. For example, for a given System 100 board, you might have it defined as an 8K Germanium Spectroscopy MCA in one file, a 1K NaI(Tl) MCA in another file, and a four-input Alpha Spectroscopy System in a third file. Before you start an experiment you simply pick the configuration you want to use.

Because an MCA definition file can include any or all of the MCAs that are available to your system, you can use more than one MCA at a time. However, each MCA can be included only once in a given definition file and each MCA in that file must have a unique name.

### Using the MCA Definition Files

To use an MCA Definition, it must first be a file; that is, you must have saved the definition to disk. Once you've done that, all you have to do is load that file into Genie-2000's internal MCA Runtime Configuration Database. From that point on all MCA operations will use the configuration information that was stored in the Definition File. To change to a new configuration, all you have to do is replace the database contents with a new file

### Starting the MID Editor

Start the MCA Input Definition Editor (MID) by double clicking on its icon in the Genie-2000 Program Group. The result will be the application window shown in Figure 6.

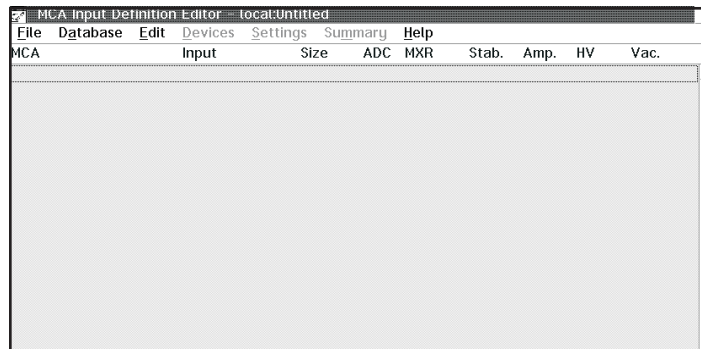


Figure 6 The MID Editor Window

Note that the Title Bar displays the name of the file you're currently working with. In the phrase "local:Untitled", "Untitled" means that no file is currently open and "local" means that the MID Editor is connected to the local VDM; this is the default condition in a non-networked environment. In an environment with multiple VDMs, you'll use **File | Node Connect** to specify which VDM is to be connected to the MID Editor for configuration purposes.

## Building an MCA Definition

In this section we'll explain how to add (and delete) the MCA entries and will explain what the definition entry consists of, then we'll explain what Defining an MCA means in general. The next several sections cover the specific definition process for each of the MCAs supported by Genie-2000.

The remainder of this chapter discusses how the definition is saved to a disk file, how a definition can be edited, and how to use a definition by loading the file into the MCA Runtime Configuration Database.

## Adding an MCA

The Edit menu, shown in Figure 7, is used to add MCA hardware to or delete MCA hardware from an MCA Input Definition. Note that the Delete MCA command is initially disabled, since the command has no meaning until there is at least one entry in the definition.

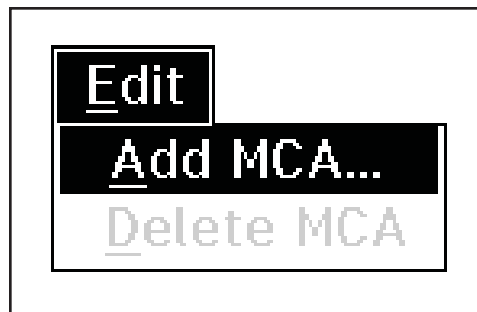


Figure 7 The Edit Menu

We'll begin our input definition by adding some MCAs. To do that, click on the **Add MCA** command in the **Edit** menu, which will pop up the "Add MCAs to Definition Table" Dialog Box in Figure 8, a typical Add MCA list box.

The Add MCA list box shows the MCAs grouped by board type. Clicking on the '+' next to a board type lets you choose a specific MCA.

Note: Figure 8 shows the MID Editor's Add MCA dialog for Genie 2000 V2.1 and later. Earlier versions of the MID Editor do not group MCAs by board type.

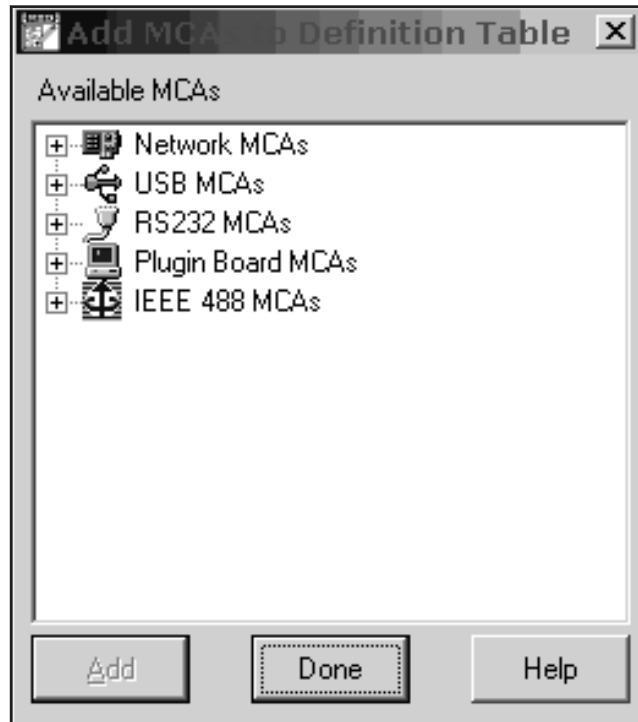


Figure 8 The Add MCA Dialog

To add an MCA to your definition, you can:

1. Click on your choice, then click on the **Add** button, or
2. Double click on your choice.

Either way, you'll see an entry added to the MCA Definition Table for each such selection you make. When you've finished selecting the MCAs you want to include in this definition, click on the **OK** button to return to the main MID window.

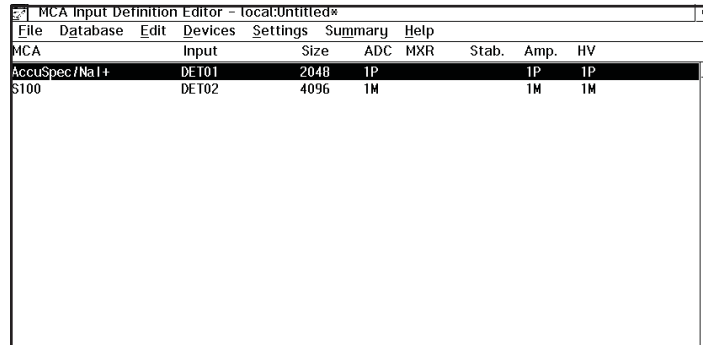
Figure 9 shows the result of using this process to add a System 100 MCA and an AccuSpec/NaI Plus MCA to the Definition Table. Please remember that this display, as well as many others in this chapter, are examples of what you *might* see; your display may not be identical.

## Interpreting the Definition Entry

As you can see in Figure 9, adding the entry put more than just the name of the MCA in the definition table. We'll take a brief look at the other items in the entry now. As we get further into the definition process we'll cover them in greater detail. Note the

## Historical MCA Input Definitions

letter following the unit number in each Definition Table item: an M indicates a manually controlled unit, and a P indicates a programmable unit.



The screenshot shows a window titled "MCA Input Definition Editor - local:Untitled\*" with a menu bar (File, Database, Edit, Devices, Settings, Summary, Help) and a table. The table has columns for MCA, Input, Size, ADC, MXR, Stab., Amp., and HV. Two rows are visible: one for AccuSpec/NaI+ and one for \$100.

MCA	Input	Size	ADC	MXR	Stab.	Amp.	HV
AccuSpec/NaI+	DET01	2048	1P			1P	1P
\$100	DET02	4096	1M			1M	1M

Figure 9 Two MCAs Have Been Added to the Table

### MCA

This is the type of MCA device being used for this particular entry in the table.

### Input

This is the name that will be used to refer to this specific hardware entry in the table. The MID Editor automatically assigns these names sequentially as DETnn, starting with nn=01. As we'll see in the "Input" section for your specific MCA type, you can easily change these names to something you find more meaningful.

### Size

This is the number of data channels assigned to this input.

### ADC

The number and types of ADCs associated with the MCA are shown here.

### MXR (Mixer/Router)

This column is used to display the current status of any Mixer/Router (also called Analog Multiplexer or AMX), if any, associated with the MCA.

### Stab. (Stabilizer)

This column shows the type of Stabilizer associated with the MCA.

### Amp

This column shows the type of amplifier associated with the MCA.

## HV

This column shows the type of High Voltage Power Supply associated with the MCA.

## Deleting an MCA

To remove an MCA from the definition, click on the MCA line you want to delete, then select the **Edit | Delete MCA** command to see the Delete MCA dialog box in Figure 10. Clicking on **OK** removes the MCA from the definition.

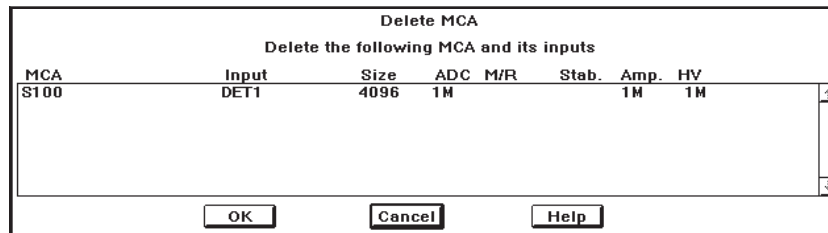


Figure 10 The Delete MCA Dialog

## Defining an MCA

Once an MCA has been added to the Input Definition Table, defining the MCA is a two step process.

### Assigning the Devices

First we use the Devices Menu to tell the system about the MCA's front end electronics. Here we define the physical hardware information, such as board number, ICB module address or Ethernet address, baud rates, sample changer connections, and so forth. You'll see that not all of the Device Menu's choices are enabled because what's offered here depends on the MCA we selected in "Adding an MCA" on page 8.

### Setting the Controls

The second step is to use the Settings Menu to define the settings for the physical devices selected in the Device Menu. For example, we can use this menu to set the amplifier, ADC and high voltage controls. Again, the menu items you're allowed to choose from depend on the MCA you're setting up. For instance, you can't set the gain for an amplifier that doesn't have a programmable gain control. Most of the settings defined here are simply the initial values to be used when the MCA is later "opened" for use. Many of the settings can be adjusted from within the Acquisition and Analysis application as the need arises. These changes can then be saved for future use, if you like.



### The Apply to All Button

The Apply to All button is used to apply the Device screen's parameter settings to all inputs defined for the current MCA.

### The Specific MCAs

Because each of the various types of MCAs that can be used with Genie-2000 has a slightly different definition procedure, we've included an installation section for two older MCAs supported by Genie-2000. For information on how a one of these MCAs is defined, read one of the following:

- "Defining an AccuSpec MCA" on page 12.
- "Defining a System 100 MCA", on page 22.

Note: If you are installing one of Canberra's newer MCAs, refer to that unit's MCA's manual for details.

To get a full understanding of all of the MID editor's functions after you have installed your MCA, read the remainder of this chapter, starting with "Saving the Input Definition" on page 31.

## Defining an AccuSpec MCA

This section discusses setting up an AccuSpec MCA. If you aren't installing an AccuSpec MCA, you should go on to the section which covers your MCA.

The AccuSpec/NaI Plus was chosen as the example for this tutorial because it has a fully programmable front end. That is, its Amplifier, ADC, and HVPS are all controlled from the PC rather than with front panel knobs and switches. Other AccuSpec MCA's are defined in a similar way.

To begin, click on the **AccuSpec/NaI+** entry in the Definition Table to select it as the MCA that is to be set up.

### Device Setup

The Device menu sets the parameters for the system's hardware, starting with the MCA itself. There is a command in the **Device** menu, shown in Figure 11, for each of the hardware sections of the MCA. The disabled (grayed) commands do not apply to the MCA currently being set up.

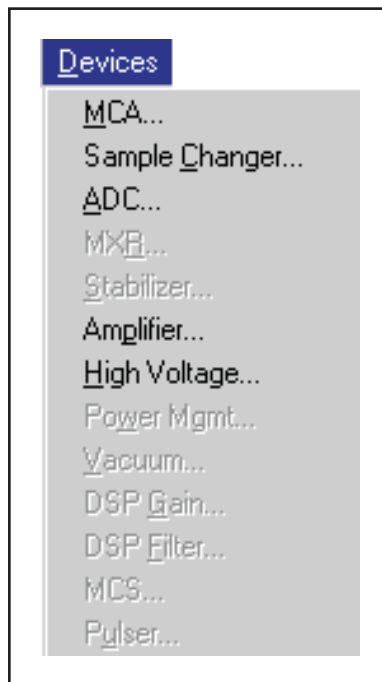


Figure 11 The Device Steup Menu

## MCA

The **MCA** command in the **Device** menu pops up the Dialog Box shown in Figure 12.

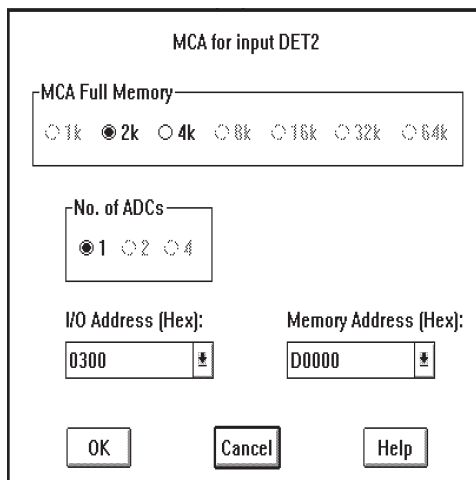


Figure 12 The MCA Device Setup Dialog

### Full Memory and Number of ADCs

The Number of ADCs is fixed, since a single ADC system is the only configuration offered for the AccuSpec/NaI Plus. Full memory size may be selected as 2K or 4K.

### I/O Address

Since there can be multiple AccuSpec boards installed in your system, you must specify the I/O Address for each board you want to use. You'll find address information for each type of AccuSpec board in "Installing AccuSpec Boards", starting on page 45.

### Memory Address

Data is read from and written to your system's AccuSpec boards through a "window" in the computer's memory. The default address (D0000) is best for most situations; if you need to change the address, refer to "Selecting a Memory Address" on page 46.

## Sample Changer

If you're going to be using a **Sample Changer**, select that command from the **Device** menu to see the Dialog Box shown in Figure 13.

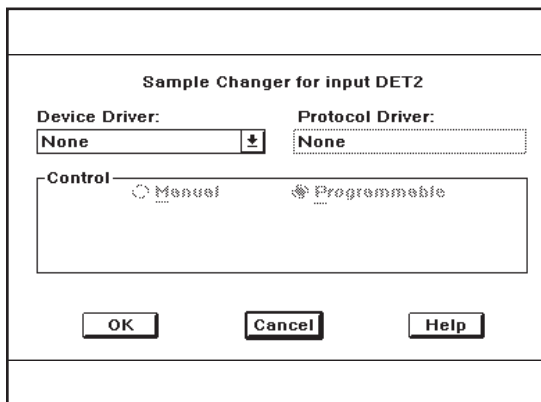


Figure 13 The Sample Changer Controls

### Device Driver

Initially this is set to None, indicating that no Sample Changer is going to be used. To change the setting, click on the Down Arrow then click on the **LPT Sample Chgr** entry in the list. When you do that, the Dialog Box will change to look like the one in Figure 14.

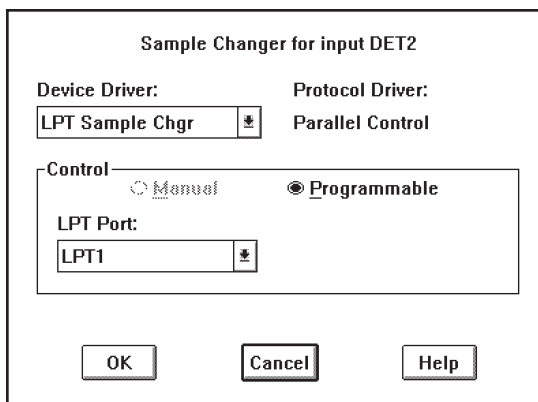


Figure 14 The LPT Sample Changer Controls

### Control

Only **Programmable** control is offered, since that is the only type of Sample Changer control available with the AccuSpec, but you do have a choice of the LPT Port which will be used.

The AccuSpec Sample Changer interfaces to the PC through a parallel (LPT) printer port, and the Drop Down list labeled **LPT Port** allows you to specify which port it is attached to. Click on the Drop Down Arrow, then click on your choice for the port.

### ADC

Since the AccuSpec/NaI Plus can only use the internal ADC, you don't need to use this command.

### Amplifier

Since the only amplifier which can be used with the AccuSpec/NaI Plus is the internal unit, there is no need to use this command.

### High Voltage

The **High Voltage** command, shown in Figure 15, specifies which type of High Voltage Power Supply you'll be using for the Detector bias.

### Device Driver

This box lets you specify whether you'll be using the built-in programmable HVPS or an external manually-controlled HVPS. Click on the Drop Down Arrow and choose the appropriate type from the list.

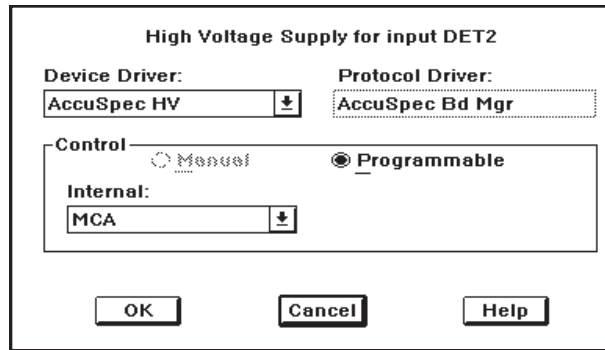


Figure 15 The High Voltage Device Dialog

### Control

This section is really for information purposes only, and will change from **Programmable** to **Manual** if you choose an external manual HVPS rather than the built-in programmable unit.

### The Settings

The commands in the Settings menu, shown in Figure 16, set the MCA's operating parameters. Since not all AccuSpec MCAs have completely programmable front ends, each of the sections which follow will be labeled with versions of the AccuSpec for which they are appropriate. Front end devices which are disabled (grayed) don't have any programmable controls.

Note that many of the parameters can also be adjusted from within the Acquisition and Analysis application. The following descriptions of each parameter specify which controls can be changed only from the MID Editor.



Figure 16 The Settings Menu

## MCA

As Figure 17 shows, the AccuSpec/NaI Plus does not have any adjustable MCA controls.

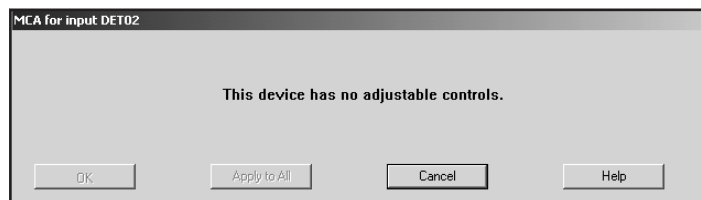


Figure 17 No Adjustable Controls Dialog

## ADC (AccuSpec/A, /NaI, and /NaI Plus)

Click on **ADC** to see the Dialog Box shown in Figure 18, which is used to set the initial operating parameters for the AccuSpec/NaI Plus's programmable ADC.

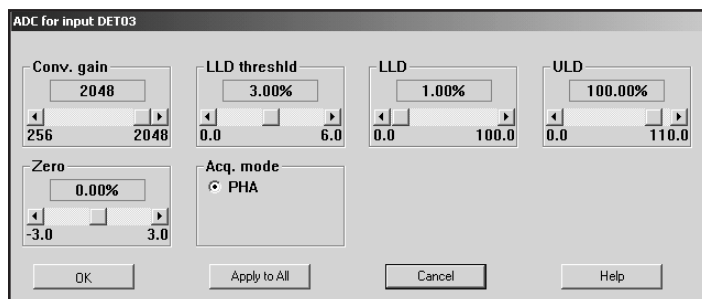


Figure 18 Controls for the Programmable ADC

Since many of the ADC's Scroll Bar controls may need to be changed often in the course of daily work, they can be adjusted both here and in the Acquisition and Analysis application. The Acquisition Mode, however, is not usually changed during the course of data acquisition, so it can only be changed here.

### Conv. Gain

This control sets the Conversion Gain of the ADC. Clicking either on the arrows at the ends of the Scroll Bar will change the gain by a factor of two.

### LLD Threshold

The ADC's threshold can be set from 0.00% to 6.0% of the ADC's full scale input.

### LLD

The ADC's Lower Level Discriminator (LLD) can be set from 0.0% to 100.0% of the ADC's full scale input.

### ULD

The ADC's Upper Level Discriminator (ULD) can be set from 0.0% to 110.0% of the ADC's full scale input.

The window between the ULD and the sum of the LLD Threshold and the LLD limits the energy range to be considered by the ADC. For example, setting the ULD at 90%, the LLD Threshold at 3.0% and the LLD at 10.0% means that only the pulses between 13.0% (3.0% plus 10.0%) and 90% of full scale will be converted by the ADC.

### Zero

This control sets the ADC Zero over the range of  $-3.0\%$  to  $+3.0\%$  of full scale.

### Acq. Mode

The AccuSpec/NaI Plus offers only the PHA acquisition mode. (AccuSpec/A and /NaI offer both PHA and SCA, which can be chosen by clicking on the appropriate button. This control can only be changed here.)

## Amplifier (AccuSpec/NaI Plus)

The **Amplifier** command is used to establish the initial settings for the programmable amplifier in the AccuSpec/NaI Plus much like the ADC command was used for the ADC. The Dialog Box is shown in Figure 19.

While the Input Polarity for the Amplifier can be set in this menu only, the Coarse and Fine Gain Controls can also be set from within the Acquisition and Analysis application if it's necessary to adjust the amplifier during data acquisition.

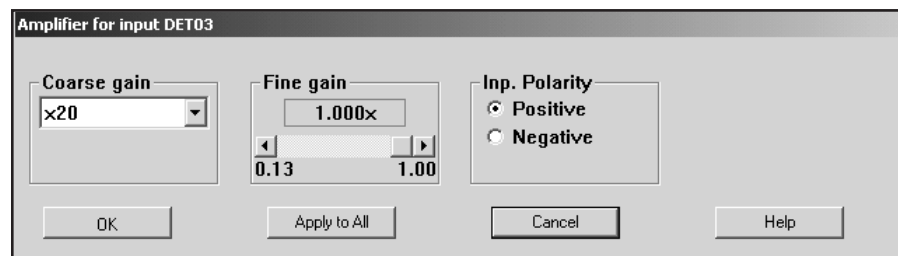


Figure 19 Controls for the Programmable Amplifier

### Coarse Gain

The Amplifier's **Coarse gain** setting is selected from the drop down list.

### Fine Gain

The **Fine gain** control, which is set by a Scroll Bar, multiplies the Coarse Gain setting by the chosen coefficient to yield the final gain setting of the Amplifier.

### Inp Polarity

The **Inp Polarity** control sets the amplifier's input polarity to positive or negative.

## High Voltage (AccuSpec/NaI Plus)

The **High Voltage** command, shown in Figure 20 provides the High Voltage Power Supply (HVPS) adjustments.



### Voltage Limit

The **Volt. limit** control establishes the HVPS's maximum output voltage. It *must* be set before the Voltage control is adjusted. This control can be set only in this Dialog Box; it cannot be changed in the Acquisition and Analysis application.

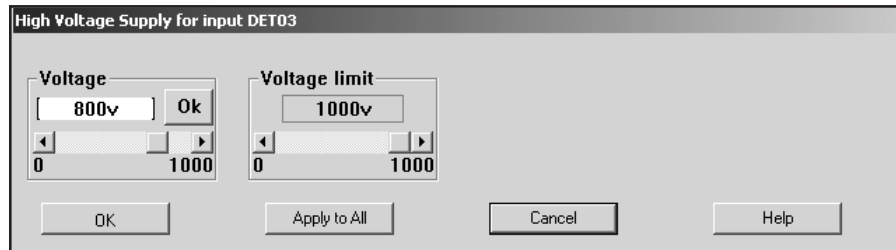


Figure 20 Controls for Programmable HVPS

### Voltage

After setting the Voltage Limit, the **Voltage** scroll bar sets the output of the HVPS anywhere between zero and the Voltage Limit (the voltage can also be set from the keyboard, then accepted with the Ok button within the control). The Acquisition and Analysis application allows you to change the output voltage, as well as turn the HVPS on and off.

### MCS (AccuSpec/FMS)

The MCS setting (Figure 21) provides a single control (Disc. Mode) with three choices: ROI, TTL, and PHA.

TTL is used when the signals to be counted are from an external source. ROI is “normal” MCS operation, with discrimination. PHA is “special” and will be used on a temporary basis within the Acquisition and Analysis windows. Refer to “Adjust” in the “Gamma Acquisition and Analysis” chapter of the *Genie 2000 Operations Manual*.

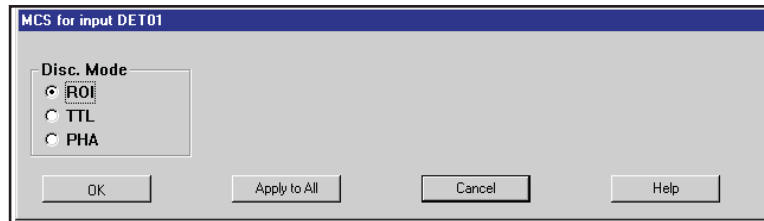


Figure 21 The MCS Input Dialog

## Input

The **Input** command is used to change the name of the Input and set up the structure of its memory via the Dialog Box shown in Figure 22. These commands are not available in the Acquisition and Analysis application.

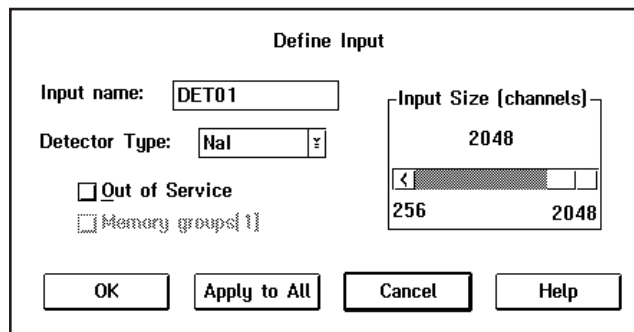


Figure 22 The Define Input Dialog

### Input Name

The default DETnn name is initially assumed as the name for your Input. But since it is displayed in a Text Input box, you can easily change the name by clicking on the current name to select it, then typing in the new name, which can be up to eight characters long. This is the name by which the detector is referred to in all applications.

### Detector Type

Use this drop-down list to select the type of detector to be used with this MCA; this also assigns appropriate default values to the spectrum display and analysis parameters.

### Input Size

This parameter is normally set to the same number of channels that you selected during the Device setup of the MCA on the assumption that you'll be using "Full Memory" for your data acquisition.

### Out of Service

Select the Out of Service Check Box when the MCA or its front end electronics are temporarily disconnected from the system. Though the MCA will still be listed in your MCA Definition File, it will not be available for data acquisition.

### Memory Groups

This Check Box is used with the Input Size control to logically segment the Full Memory of the MCA into Halves, Quarters, and so forth. Note that this control is disabled when this ADC is associated with a Mixer/Router. Using it is a two step process:

1. First you must use the Input Size control to set the acquisition memory size to less than the Full Memory size of the MCA. For example, set to 1024 instead of the Full Memory size of 2048.
2. Enable Memory Groups by clicking on the Check Box. When you do that, the number of available groups will be displayed in the brackets to the right of the control. Using our 1024 out of 2048 example again, the number 2 would appear; the MCA is now set up to acquire 1024 channels of data into either half of its memory.

## Defining a System 100 MCA

If you're not installing a System 100 MCA, go on to the section which covers your MCA.

### Device Setup

Device setup covers setting the parameters for the system's hardware, starting with the MCA itself. Clicking on **Device** in the Menu bar shows the menu in Figure 23. There is a command in the menu for each of the hardware sections of the MCA. The disabled (grayed) commands do not apply to the MCA currently being set up.

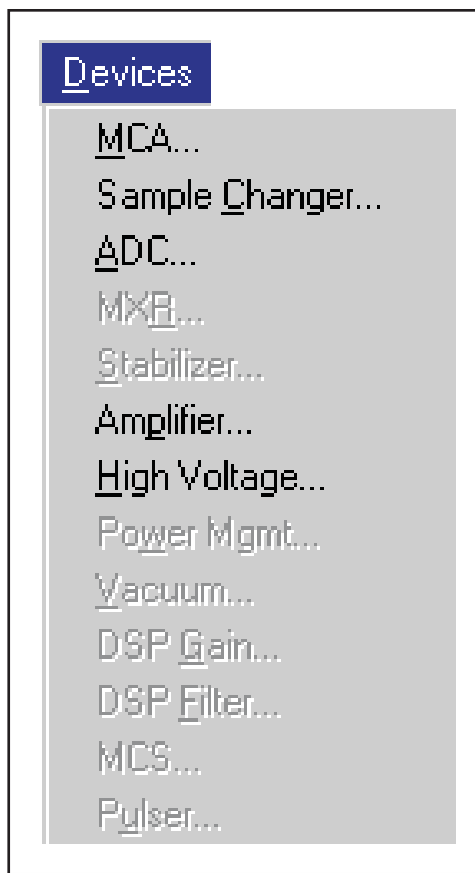


Figure 23 The Device Settings Menu

## MCA

Selecting the **MCA** command from the menu yields the Dialog Box shown in Figure 24, which is used to set the more global aspects of the MCA.

### Full Memory

Buttons are used to select just how much of the available MCA memory you want to use. As shown in Figure 24, only 4K (4096 channels) of the available 16K channels are going to be used.

### Number of ADCs

This box sets the number of ADCs for those MCAs that can have more than one. Since the System 100 can only have one ADC, that's the only choice that is offered and it has been selected.

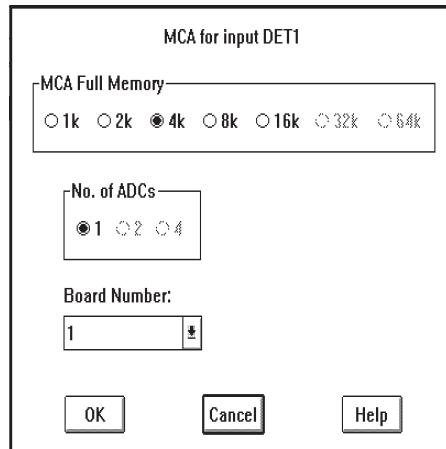


Figure 24 The MCA Device Dialog

### Board Number

Up to four System 100 MCA boards may be installed in your PC. This parameter is used to tell the system which board you want this MCA definition to refer to. Select the required System 100 board by clicking on the Drop Down arrow, scrolling down the list to locate the board you want to use, and then clicking on it.

### Sample Changer

The next command, **Sample Changer**, is used to set up the MCA's Sample Changer control; it can be ignored if you're not using a Sample Changer. But if you do want to include sample changer control in your MCA, clicking on the command will pop up the Dialog Box in Figure 25.

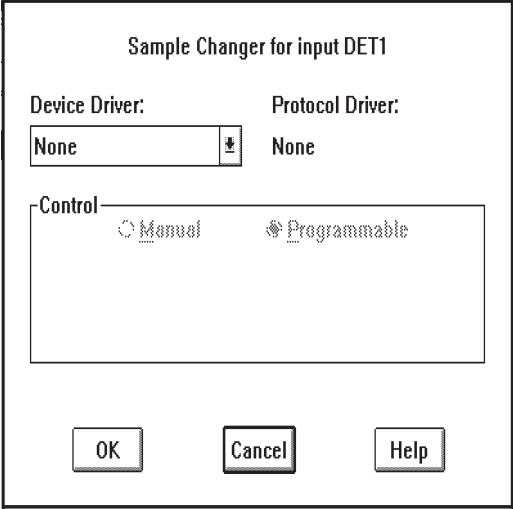


Figure 25 The Sample Changer Dialog

**Device Driver**

What this really means is “What kind of Sample Changer do you want to use?”, and you select the type via a standard Drop Down list. Since we’re setting up a System 100, that’s the type you’ll probably want to use. Click on that choice in the Drop Down list to select it. When you do, you’ll see the Dialog Box change to look like the one shown in Figure 26.

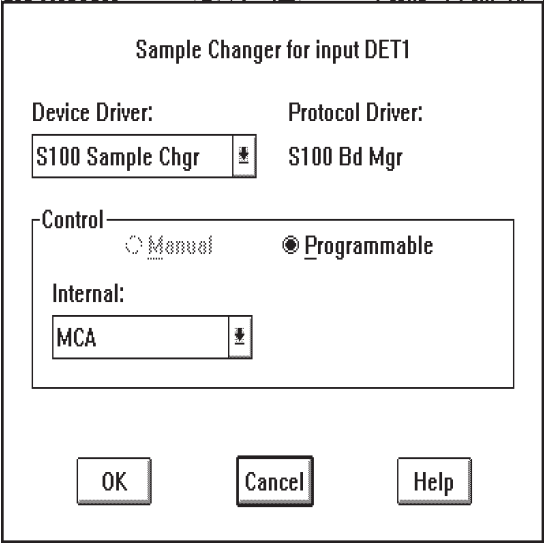


Figure 26 The Sample Changer Controls

## Control

The Control of the Sample Changer was immediately set to Programmable because that's the only type of Sample Changer the System 100 supports. In addition, there's a Drop Down list labeled Internal that's currently set to MCA to let you know that the program which will control the Sample Changer will be under the control of the MCA's internal control logic. If you click on the Drop Down arrow, you'll discover that there are no other choices offered, since that's the only type of control logic that can be used with the System 100's Sample Changer.

The next two sections, **ADC** and **MXR** are only applicable if you're going to be using a Mixer/Router (also called Analog Multiplexer or AMX) with the System 100 MCA board. If you are not going to be using one, you are finished with the Device setup of the System 100. While there are still two commands remaining in the Device menu – Amplifier and High Voltage – they are only applicable to programmable front ends. Since the System 100 uses manually controlled Amps and Power Supplies, the commands are not needed to complete the setup.

## ADC

Next in the **Device** menu is the **ADC** command, which shows the Dialog Box in Figure 27.

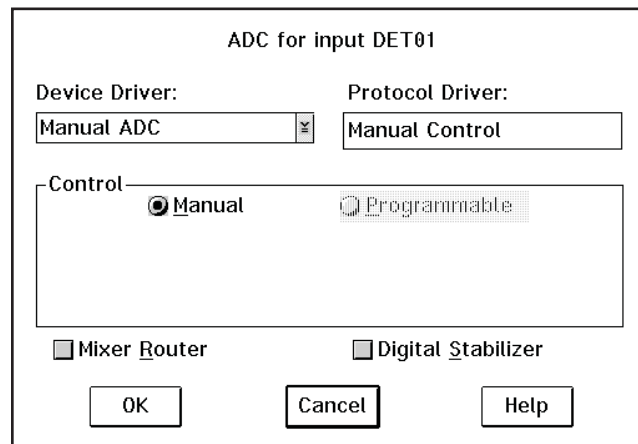


Figure 27 The ADC Device Dialog

Since the System 100 only uses a single manually controlled ADC, you can choose whether you're going to use a Mixer/Router (also called Analog Multiplexer or AMX) or a Stabilizer with it. If you choose Stabilizer, you'll notice that there are no selections to make under Stabilizer in the Device menu.

If you enabled a Mixer/Router, you'll notice that the MXR column of the System 100 entry in the MCA Definition Table now contains the entry 1-1M. This means that a Mixer/Router has been selected, is currently set to only one input, and the Mixer/Router is of the Manual control type.

### MXR (Mixer/Router)

If you selected the Mixer/Router, choose the **Device | MXR** command to bring up the Dialog Box in Figure 28.

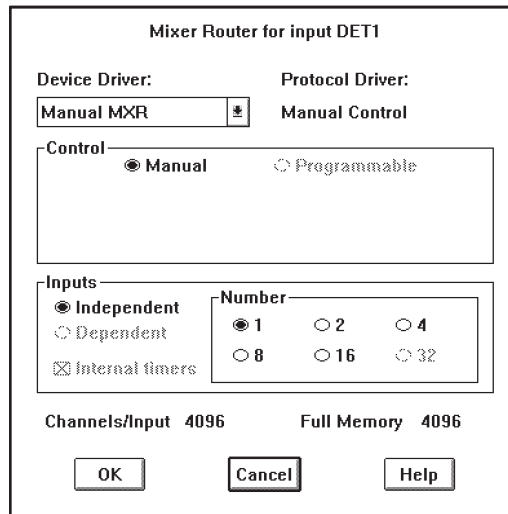


Figure 28 The MXR Device Dialog

### Inputs

This dialog box sets up the number of inputs that are going to be used, which you do by clicking on the appropriate button. Note that as you change the number of inputs, the Channels/Input display will be automatically updated for you.

A Mixer/Router (also called Analog Multiplexer or AMX) always uses all of the full memory, which is divided evenly between the selected number of inputs. The minimum number of channels which can be assigned to an input is 256.

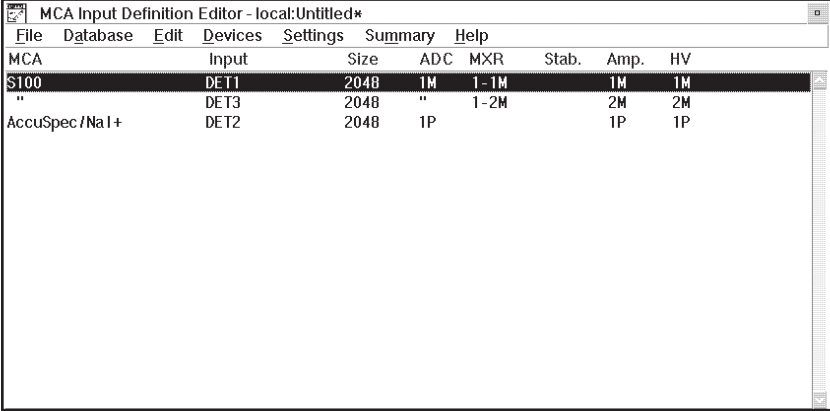
Note that the memory groups are not allowed to be used in conjunction with multiplexed inputs.

### The Updated Definition Table

If you had decided to use two inputs on the Mixer/Router, exiting the Dialog Box via **OK** would result in a Definition Table like the one shown in Figure 29.



The first thing you'll probably notice is that an "extra" Input has been added to the table, a System 100 called DET03. This was done to allow you to refer to each of the Mixer/Router's inputs as logically separate entities even though they happen to be sharing the same physical MCA board.



MCA	Input	Size	ADC	MXR	Stab.	Amp.	HV
S100	DET1	2048	1M	1-1M		1M	1M
	DET3	2048	"	1-2M		2M	2M
AccuSpec/NaI+	DET2	2048	1P			1P	1P

Figure 29 The Updated Definition Table

In addition, the MXR column for the entries indicates which of the Mixer/Router's inputs is associated with which logical Input.

### Amplifier and High Voltage

The Amplifier and High Voltage Device screens offer no selectable options for the System 100 MCA.

### The Settings

The commands in the Settings menu, shown in Figure 30, set the MCA's operating parameters. Since the System 100 uses only manually controlled front ends only two commands – MCA and Input – are enabled.



Figure 30 The Settings Menu

Note that for many of the parameters, the initial values entered during Settings can be adjusted as necessary from within the Acquisition and Analysis application. The following descriptions of each parameter specify which controls can be changed only from the MID Editor.

## MCA

Selecting the **MCA** command pops up the Dialog Box shown in Figure 31. To change the acquisition mode, click on the Drop Down arrow, scroll to the mode you want to use, and click on it. If you're using a Mixer/Router (also called Analog Multiplexer or AMX), the mode you select will apply to *all* of the Mixer/Router's inputs. Note that the mode can be also be changed from within the Acquisition and Analysis Acquisition and Analysis application.

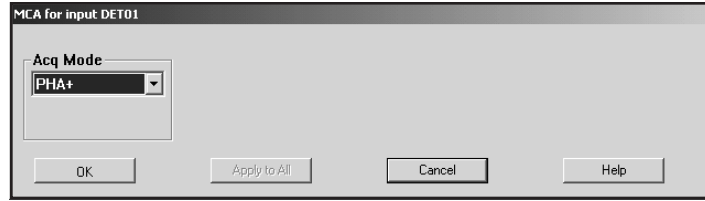


Figure 31 The MCA Sttings

## Input

The **Input** command is used to change the name of the MCA and set up the structure of its memory via the Dialog Box shown in Figure 32. These commands are not available in the Acquisition and Analysis application.

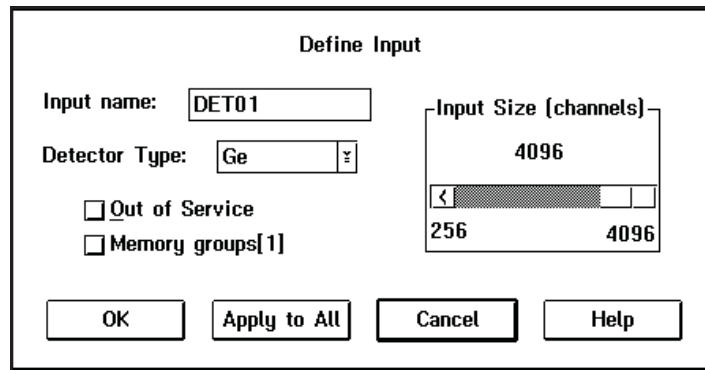


Figure 32 Define Input Dialog

## Input Name

The default *DETnn* name is initially assumed as the name for your MCA. However, since it is displayed in a Text Input box, you can easily change the name by clicking on the current name to select it, then typing in the new name, which can be up to eight characters long. This is the name by which the detector is referred to in all applications.

**Detector Type**

Use this drop-down list to select the type of detector to be used with this MCA; this also assigns appropriate default values to the spectrum display and analysis parameters.

**Input Size**

This parameter is normally set to the same number of channels that you selected for use during the Device setup of the MCA on the assumption that you'll be using "Full Memory" for your data acquisition. To use less than the maximum available memory size, slide the Scroll bar to select the size you want to use.

**Out of Service**

Select the Out of Service Check Box when the MCA or its front end electronics are temporarily disconnected from the system. Though the MCA will still be listed in your MCA Definition File, it will not be available for data acquisition.

**Memory Groups**

This Check Box is used with the Input Size control to logically segment the Full Memory into halves, quarters, and so forth. Note that this control is disabled when this ADC is associated with a Mixer/Router. Using it is a two step process:

1. First you must use the Input Size control to set the acquisition memory size to less than the Full Memory size of the MCA. For example, set to 1024 instead of the Full Memory size of 4096.
2. Enable Memory Groups by clicking on the Check Box. When you do that, the number of available groups will be displayed in the brackets to the right of the control. Using our 1024 out of 4096 example again, the number 4 would appear; the System 100 is now set up to acquire 1024 channels of data into any of the four Quarters of its memory.

When we take a look at data acquisition in the next chapter you'll see that each group can be treated as an individual entity in the same way that a traditional MCA's memory can treat Halves, Quarters, and so forth, as individual entities.

## Saving the Input Definition

Having completed our definition, the next step is to save it in a disk file so we can use it in the future. To remind you that you need to do this, you'll see an asterisk (\*) in the Title Bar, next to the name of the current definition. The asterisk means that the definition has been changed but not yet saved. To save your definition, click on the **File** menu's **Save** command. When you do that, you'll see the Dialog Box shown in Figure

**CAUTION** If you have changed an existing Input Definition, saving it will set its calibrations to default and will clear the Acquisition Start time.

## Save and Save As

Even though you selected the Save command, you'll notice that the Dialog Box is labeled Save As. This is because the Save command is really a "Replace the old version with a new one" command, and we don't have an "old version" of our table to replace (ours is still labeled "Untitled", which means it has never been Saved). The system realizes this and automatically pops up the Save As Dialog Box so we can assign a name to our table.

## Using Save As

Since the word Untitled displayed in the File Name Text Input box is already highlighted, all you have to do to replace it is type a file name, then press the TAB key to move to the File Descriptor input box.

### The File Descriptor

The text cursor is now located in the input field called File Descriptor. This a 32-character description that is stored with your file to make it easier to locate it when you want to use it again.

## Changing the Summary View

Before going on to see how to edit an existing Input Definition Table, one that you've built previously and saved to disk, there's one more menu to look at. This is the Summary menu, which is shown in Figure 33.

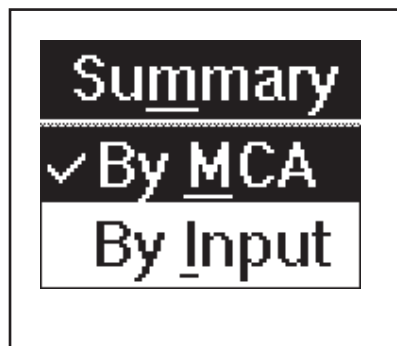


Figure 33 The Summary Menu

The **Summary** menu has two commands: **By MCA** and **By Input**, which change the order in which the information in the Input Definition Table is displayed. **By MCA** means that the first column of the table will display the MCA type that is being used for each entry. If you choose **By Input**, the MCA and Input columns will be reversed in the display and the Inputs will be sorted alphabetically.

You can choose either method, but in the case of systems with a large number of inputs, “By Input” is an easier display to understand than “By MCA”.

## Editing an MCA Definition

The procedures that we used in the previous sections can also be used to edit MCA Input Definitions that have already been saved to disk.

### Opening an Input Definition File

To edit a file that has not been loaded into the MCA Runtime Configuration Database, all you have to do is read it into the Input Definition Editor with the **File** menu’s **Open** command.

If you have already loaded the definition into the MCA Runtime Configuration Database, it must first be unloaded before it can be opened in the editor. See “Unloading the Database” on page 36 for the procedure to use.

### Looking at the File Details

If you’re not sure which file you want to edit, click on the name of the file that you think is the correct one, then click on the **Info** button to see further information about the file. Doing that will pop up the Dialog Box shown in Figure 34.

The key piece of information here is the File Descriptor, which is the “extended file name” that you added when the file was originally saved. From this you should better be able to determine if the file you selected is the one you want.

When you’re finished with the file details, click on **OK** to return to the Open Dialog Box. Now you can either click on the **Open** button to open the file you selected or select a different file and view its details.

### Editing the Definition

All of the menus and commands available for defining an MCA are also used for editing a definition. Just click on the entry you want to change and apply the commands as before. When you’ve finished editing the definition, **Save** it. Note that you can’t edit a

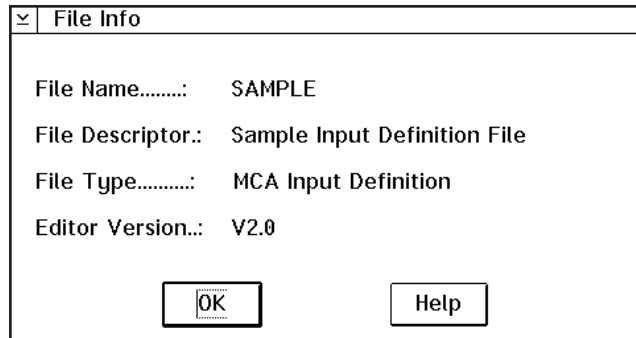


Figure 34 The File Info Display

database which is being used by the Runtime Database; you'll first have to unload it first, as described in "Unloading the Database" on page 36).

## The New Command

If you want to create a totally new MCA Definition, the **File** menu's **New** command clears the definition table so you can begin a new definition.

Because New is a destructive operation, selecting it will cause the program to ask for a confirmation in one of two ways:

1. If the Definition currently being displayed has not been changed since it was last saved (no asterisk in the Title Bar), you will be asked if you want to erase the current Definition. Click on **OK** to erase it, or **Cancel** to return to the Input Definition Editor.
2. If the Definition currently being displayed has been changed but *not* saved, you will be given a chance to save it.

## The Input Definition Report

The **File** menu's **Report** command always saves to a disk file, but if you click on **Yes** in the dialog box that pops up, you can send the report to a disk file *and* print the report as well. Click on **No** to save it to a disk file without printing the report.

## Using MCA Definition Tables

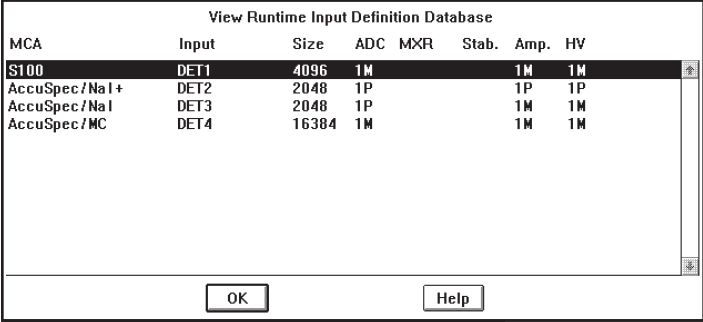
The whole purpose behind building MCA Input Definitions is to let Genie-2000 know the number and types of MCAs you'll be using with your system. You do this by load-

ing one or more MCA Definition Files into the MCA Runtime Configuration Database.

This database is shared by all Genie-2000 programs and is used by those programs to gain access to the actual MCA hardware in your system. In this section we'll take a look at the procedures used for setting up that database.

## Looking at the Current Database

To see the current contents of the database, click on the **Database** menu's **View** command, which will pop up the display shown in Figure 35. Click on a line in the list, then use the Device and Settings menus to look at the details of that definition. Click on **OK** to close the View window.



The screenshot shows a window titled "View Runtime Input Definition Database" with a table of MCA definitions. The table has columns for MCA, Input, Size, ADC, MXR, Stab., Amp., and HV. The first row is highlighted.

MCA	Input	Size	ADC	MXR	Stab.	Amp.	HV
S100	DET1	4096	1M			1M	1M
AccuSpec/NaI+	DET2	2048	1P			1P	1P
AccuSpec/NaI	DET3	2048	1P			1M	1M
AccuSpec/MC	DET4	16384	1M			1M	1M

At the bottom of the window are two buttons: "OK" and "Help".

Figure 35 Viewing the Database

## Loading and Unloading Definitions

Before you can use an MCA Definition, you'll have to load it into the database, so we'll start with that process. Note that you can't edit a loaded database; you'll first have to unload it as described in "Unloading the Database" on page 36).

The Load/Unload functions will be disabled while any Acquisition and Analysis applications are running and have open datasources. This prevents one user from altering the runtime database while another user is accessing it.



## Loading the Database

A new Definition can be loaded into the Database with the **Load to** command, which brings up the Dialog Box in Figure 36.

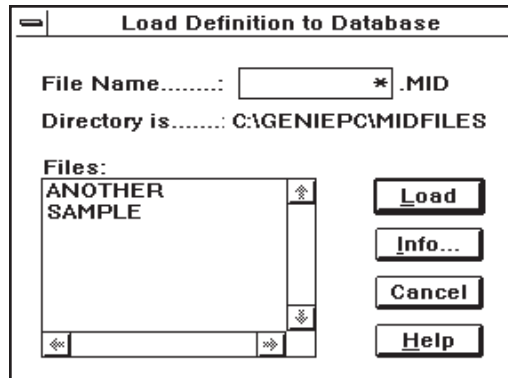


Figure 36 The Load to Dialog

### Selecting the File

This Dialog Box works just like the File Open Dialog Box, but instead of opening the file for editing, it loads the file into the database.

### Loading Multiple Definitions

Though you will usually use only one definition at a time, there may be times when you want to load more than one definition. To do this, be sure that each of the Input names in the Definition Files is unique and that any single MCA (for instance, System 100 Board #1) is defined only once. As long as both of these conditions are true, you can load as many Input Definitions as you like.

If you try to load an Input Definition which contains a duplicate Input name, the system will display a message telling you that the requested Load can't be done.

## Unloading the Database

You'll recall that while the programmable front end controls, such as ADC Gain or Amplifier Gain, are initially set with the MCA Input Definition Editor, many of them may also be adjusted from within the Acquisition and Analysis application while you're collecting data.

Any adjustments you make in the Acquisition and Analysis application can be stored in the database (with File | Save) and, when you Unload the database, are saved into an Input Definition File. This saves all of the control settings for future sessions.

### The Unload Process

To unload a Database, click on the **Database** menu's **Unload from** command, which will bring up the Dialog Box shown in Figure 37. If several choices are listed, there are multiple definitions in the database.

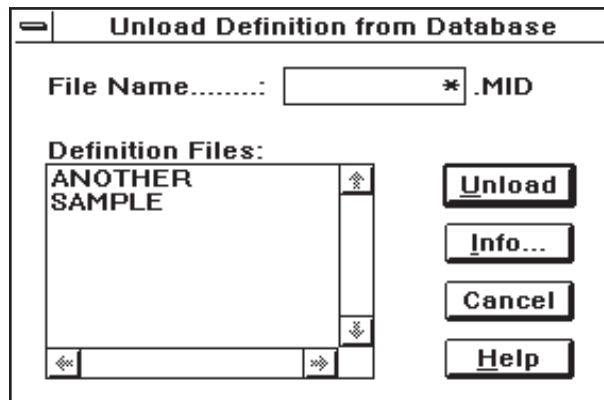


Figure 37 The Unload From Dialog

Click on the one you want to unload, then click on the **Unload from** button. Note that this menu item is disabled if the MCA Runtime Configuration Database is currently being used by another application.

## 3. Hardware Installation

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This chapter covers installation of the System 100 MCA and AccuSpec MCA hardware. AIM and InSpector MCA hardware installation is covered in their manuals. You'll need access to the PC's expansion bus and system board when installing internal options such as:

- MCA boards
- Display adapters
- Memory expansion
- I/O adapters

**CAUTION** To prevent a loss of data stored on a fixed disk drive, back up all files before altering your system.

### Installing System 100 Boards

Canberra has carefully designed the System 100 MCA boards so that there is no conflict with any IBM devices, but if another non-IBM adapter board is installed it is advisable to check its I/O addresses before installing the Canberra board. In the event of an addressing conflict, the System 100 allows for an alternate set of addresses. The System 100 boards can be one of two models. They can be distinguished by the label on chip A63: Model 4610 has a blue label and Model 4611 has a white label, as shown in Figure 38.

There is no restriction on the MCA numbering (see Table 1). For example, if there is a conflict at both the primary and alternate addresses for MCA #1, you can set up the board as MCA #2. Note that two boards can't use the same MCA number.

The System 100 does not require DMA, Interrupt, or Memory Access from the computer's bus – only INput and OUTput at the listed addresses. The required Bus Signals for both PC Bus and Micro Channel Bus MCA Boards are listed in Appendix D, *Technical Information*. The Genie-2000 software allows up to four System 100 MCA boards to operate simultaneously.

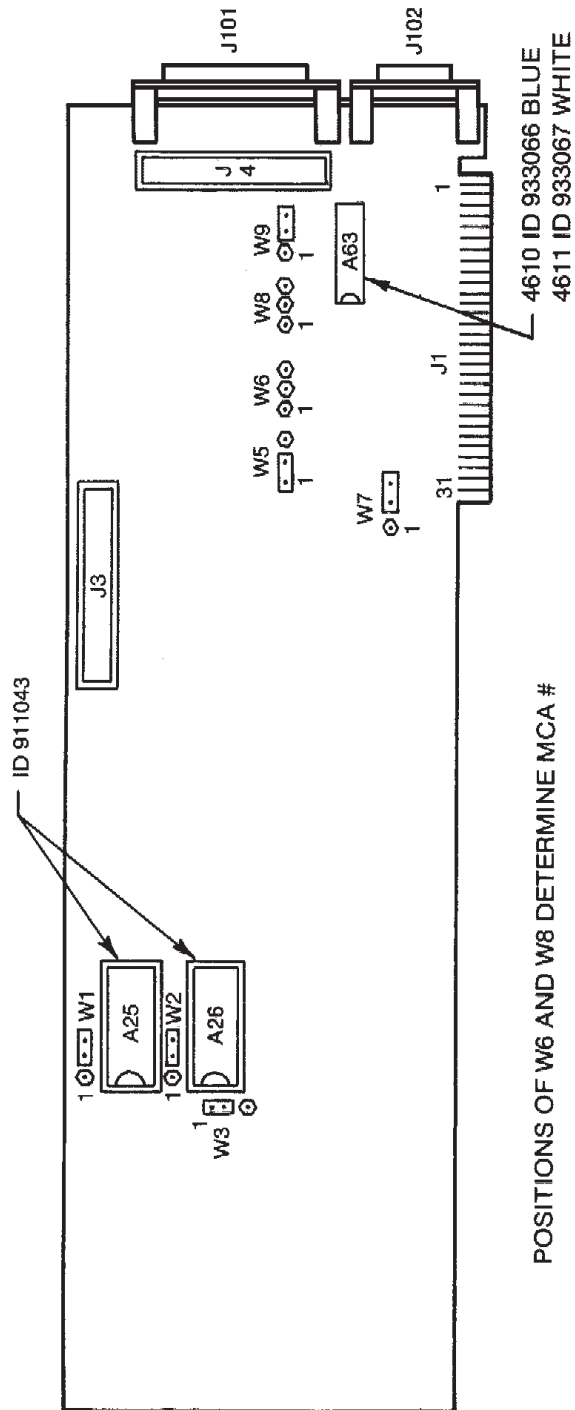


Figure 38 System 100 Board Component Location

Table 1 System 100 PC I/O Address Map

<b>Model 4610</b>				
	Jumpers		Primary Address	Alternate Address
MCA	W6	W8	W9=2-3	W9=1-2
#1	2-3	2-3	340-345 <sub>H</sub>	300-305 <sub>H</sub>
#2	2-3	1-2	348-34D <sub>H</sub>	308-30D <sub>H</sub>
#3	1-2	2-3	350-355 <sub>H</sub>	310-315 <sub>H</sub>
#4	1-2	1-2	358-35D <sub>H</sub>	None
<b>Model 4611</b>				
	Jumpers		Primary Address	Alternate Address
MCA	W6	W8	W9=2-3	W9=1-2
#1	No selection			
#2	2-3	1-2	348-34D <sub>H</sub>	308-30D <sub>H</sub>
#3	1-2	2-3	350-355 <sub>H</sub>	310-315 <sub>H</sub>
#4	1-2	1-2	358-35D <sub>H</sub>	318-31D <sub>H</sub>

## PC Bus MCAs

Two boards can't be set for the same MCA number.

Note: If there is an address conflict it will not be possible to install the System 100 board unless the other adapter is removed.

### Installing the PC MCA Board

1. Turn OFF the power to the system unit and to all connected external options (display, printer, and so forth). If this is the initial installation, refer to the documents provided with the computer. Unplug the power cord to the system unit.

Note location of all cables and disconnect them from the system unit.

2. Follow the instructions in your computer's manual on how to remove the cover.
3. Remove the rear panel expansion slot cover from one of the unused full length expansion slots. Set the screw aside for later use.
4. Install the board into the selected slot aligned so that the connector sockets are at the rear. The beveled edge of the cover bracket fits into a slot in the rear panel plate and the other end of the board should slide into a plastic support.

On some computers, it will be easier to install the MCA board if the adjacent boards' brackets are loosened. Press the board in firmly to fully seat it in its expansion bus connector.

5. Install the screw that was removed with the slot cover and secure all boards.
6. Repeat steps 3 through 5 for all boards to be installed in the computer.
7. Install the system unit's cover and tighten the cover screws.
8. Connect the AC power cord.
9. Apply the board label that was provided with the board to the rear panel slot. The MCA number should correspond to the address selected. This will help later when connecting cables.

## Micro Channel Bus MCAs

Boards designed for the Micro Channel bus have programmable registers that replace jumpers and switches. These registers are loaded during system configuration at power-on. The Adapter Descriptor File (ADF) for the board is included on the Genie-2000 Basic Spectroscopy disk. This is the same file that is on the S398 disk. If you are upgrading the software of an existing system, it is not necessary to reconfigure your system.

### Copying the S100 Configuration File

Before installing an MCA board in the computer, it will be necessary to copy the ADF file from the S400 disk to your *backup* copy of the PS/2 Reference Disk. *Do not* copy it to the original disk supplied with your PS/2 system!

The backup disk is a 1.44 MB (high density) disk that was created from the Reference Disk that came with your computer. The file to copy from the S400 disk is called "@60B2.ADF".

If DOS is installed, you can use the DOS Copy command to copy the “@60B2.ADF” file to your Backup Reference Disk.

If this is the initial installation, refer to the Quick Reference Manual supplied with your computer. The Backup Reference Disk has a “Copy an Option Disk” function. Booting the computer with the Backup Reference Disk in drive A: will bring up the menu. Follow the instructions on the screen.

### **Installing the Micro Channel MCA Board**

1. Turn power OFF to the system unit and all connected external options (display, printer, and so forth). If this is the initial installation, refer to the documents provided with the computer. Unplug the power cord to the system unit.

Note location of all cables and disconnect them from the system unit.

2. Follow the instructions in your computer’s Guide to Operations on how to remove the cover.
3. Remove the rear panel cover from one of the unused expansion slots. Loosen the thumbscrew, then slide the cover out. The System 100 Micro Channel MCA board can be plugged into any Micro Channel bus slot.
4. Install the board by pressing it firmly into the slot connector, but don’t force it into the slot (the plate is fairly flexible and will bend if not positioned properly). The notch on the rear panel plate should slide over the grounding screw.
5. Tighten the rear panel screw.
6. Repeat steps 3 through 5 for all boards to be installed in the computer.
7. Install the system unit’s cover and tighten the cover screws. Some computers have a cover lock, which can be used to protect devices and options inside the computer.
8. Connect the AC power cord.

### **Configuring the Micro Channel Computer**

The Backup Reference Disk should be inserted in drive A: Turning on the computer will cause it to recognize that its configuration has changed and an error “165” message will be displayed, followed by an IBM logo display.

Note: If the computer is turned on without the Backup Reference Disk, error “165” will be displayed and you will be prompted to use the Backup Reference Disk. Insert it in drive A: and reboot the computer by pressing CTRL+ALT+DEL.

From the IBM logo screen, press ENTER to continue. An explanation of the “165” error should appear.

1. Press the PG DN key to continue.
2. You will then be asked if “Automatic Configuration” is to be run. Answer Yes (press Y).

Note: Running this Automatic Configuration affects only the boards that have been added or removed. Boards that have not been moved will remain as previously configured.

3. Press ENTER with the disk still in drive A:. The computer should reboot; this time without error.
4. After the IBM logo screen appears, press ENTER. This time the Main Menu will be displayed.
5. Use the cursor keys to select “Set Configuration”. Then press ENTER. This will cause the Configuration Menu to appear.

Note The “Run Automatic Configuration” command configures the computer and all adapters including the System 100 MCA boards to default settings, which may not be desirable.

6. Select “View Configuration”, then press ENTER. This will show the configuration that is stored in the computer’s battery-backed memory. Press the ESC key after determining if the configuration is acceptable. If it is acceptable, go to step 12.
7. To make changes to the configuration, select “Change Configuration” and press ENTER.
8. Use the cursor keys to move to the line that you want to change.
9. For the MCA board(s), use the F5 and F6 keys to advance through the options until you have the selection you want to use. Boards can be assigned in any order; the computer will inform you of an address conflict by placing an asterisk (\*) beside boards with overlapping addresses. The conflicts *must* be resolved by selecting a different board number or alternate address. Refer to Table 2 for primary and secondary addresses.



Note Do not assign the same “MCA#” to multiple boards. The configuration program only checks for overlapping addresses, but the application program will only recognize one board of the same MCA#. You can’t have one board as MCA number *n* at the Primary address and another board with the same MCA number at the Alternate address.

Table 2 System 100 Micro Channel I/O Address Map

MCA	Primary Address	Alternate Address
#1	340-347 <sub>H</sub>	300-307 <sub>H</sub>
#2	348-34F <sub>H</sub>	308-30F <sub>H</sub>
#3	350-357 <sub>H</sub>	310-317 <sub>H</sub>
#4	358-35F <sub>H</sub>	318-31F <sub>H</sub>

10. After making the changes, press F10 to Save this configuration in the computer’s battery-backed memory.
11. Press ENTER to continue, then press ESC to return to the Set Configuration Menu.
12. You should now make a copy of the configuration on your Backup Reference Disk. Select “Backup Configuration” and press ENTER.

Note: If the contents of the battery-backed memory are lost because of battery failure, the “Restore Configuration” command in the Set Configuration Menu will transfer the saved configuration from the Backup Reference Disk to the memory.

13. Select “View Configuration”. Note which MCA# is in which slot and apply the corresponding label to the rear panel from the label set included with each MCA board. This will help later when connecting cables.
14. Press ESC to return to the Main Menu. If you are doing the initial installation, you may want to use some of the other programs provided on the Reference Disk before installing the operating system and application programs. Refer to the documentation provided with the computer.

## Installing AccuSpec Boards

Five configurations of the AccuSpec board are supported:

- AccuSpec A: 8K channel memory, 8K on-board ADC.
- AccuSpec B: 16K channel memory, no ADC.
- AccuSpec NaI: 8K channel memory, 2K on-board ADC.
- AccuSpec FMS: 18K channel memory (16k optional), no ADC.
- AccuSpec NaI Plus: 4K channel memory, 2 groups, 2K on-board ADC, Amp and HVPS.

To use the Genie-2000 system you will need the following hardware: a detector, front-end electronics, a personal computer system and an AccuSpec board or boards. These devices are connected as shown in Figure 39.

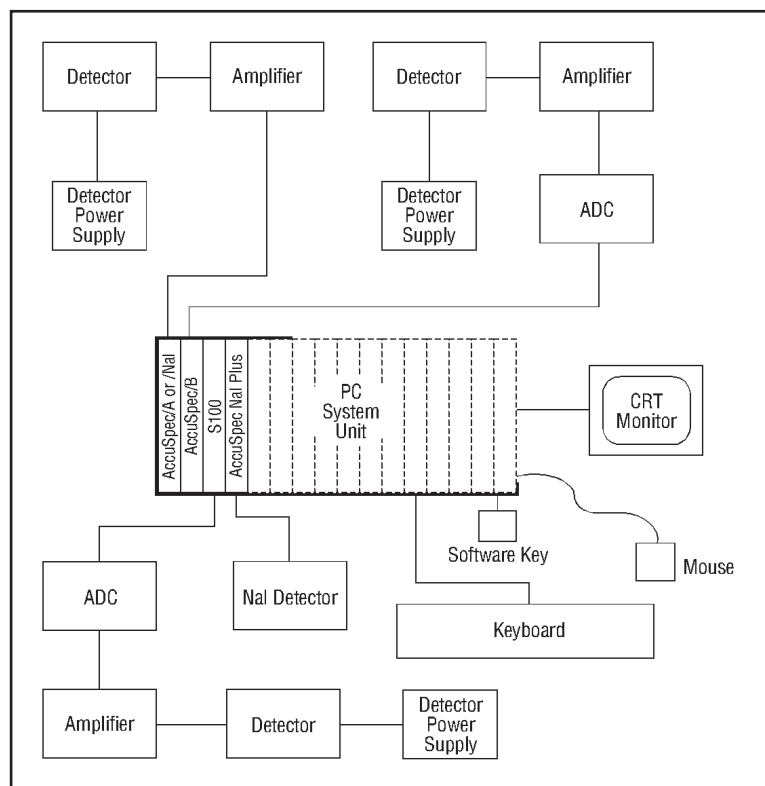


Figure 39 Standalone Genie-PC System

### Unpacking

Carefully remove all materials from the shipping container. Check all equipment for possible damage. If damage was incurred during transit, contact Canberra's Customer Service Department immediately.

For each AccuSpec B board you received, you should have an AccuSpec B ADC Interface Cable (C1704).

For each AccuSpec/NaI Plus board you received, you should have a Preamp Power Adapter Cable (C1552).

If you are going to use the ADT, AMPBSY, SCA or GATE signals from an AccuSpec A or AccuSpec NaI board, you should have a 759618 breakout cable for these signals; it must be ordered separately.

If you are going to use an AccuSpec A or AccuSpec NaI with Model 589 or Model 8224 Analog Multiplexer, you should have a 1.8 m 840617 cable or a 4.5 m 840618 cable. These cables require an additional rear panel slot on the PC.

If you intend to use a Model 589 or 8224 Analog Multiplexer, you must have a 751776 interface cable to connect the multiplexer to a parallel port on the computer (note that this port *must not* have the security key connected to it). This provides the required start/stop control.

### Selecting a Memory Address

Data is read from and written to the AccuSpec board's on-board memory through a "window" in the computer's memory address space. All boards in the system should be set to the same window address. The memory window address can be changed by running the MCA Input Definition Editor; see Chapter 2, *MCA Input Definition Editor*.

You must specify an address for the memory window which does not conflict with any other hardware in your system. The memory window normally begins at a 32K or 64K byte boundary. Each channel uses 4 bytes and a window of 64K bytes. A system memory map for Personal Computers is shown in Table 3.

ROM on I/O adapters is usually in the range C0000-CFFFF. Addresses D0000-DFFFF are free in most machines, thus D0000 is used as the default base of the AccuSpec memory window.

When choosing a memory window address for the AccuSpec board in a PS/2 computer with a VGA or better monitor, the address may need to be on a 32K boundary.

Table 3 PC System Memory Map

Address Range	Size	Name or function
00000 to 9FFFF	640K	Main system memory
A0000 to AFFFF	64K	EGA, VGA AND MCGA
B0000 to BFFFF	64K	EGA and all display adapters
C0000 to DFFFF	128K	Reserved for ROM on I/O adapter such as AccuSpec
E0000 to EFFFF	64K	64K ROM on AT, free on PC/XT.

The following table shows some possible mapping options:

PS/2 with VGA  
 C8000 (8K channel maximum)  
 D0000 (16K channel maximum)  
 D8000 (8K channel maximum)

### Selecting Jumper Options

Before installing AccuSpec boards in your computer, you must select the switch and jumper options on each board. Jumpers are factory configured for normal operation. Therefore, only the I/O address switches need to be set for most applications. Instructions for selecting basic options are given below.

NOTE: Some jumpers may be soldered to minimize the chances of invalid configurations.

## AccuSpec A and AccuSpec NaI

Specific jumpering instructions for AccuSpec A and AccuSpec NaI boards are shown in Figure 40 and Table 4.

### Base I/O Address Switches.

The Base I/O Address Switches should be set to (hexadecimal) 300, 310, 320, and 330 for units 1, 2, 3 and 4, respectively, unless other hardware interferes. The switches are labeled A4 through A10. An OFF or OPEN switch is a 1. An ON or CLOSED switch is a 0.

Switch settings for the four standard addresses are shown in Table 4.

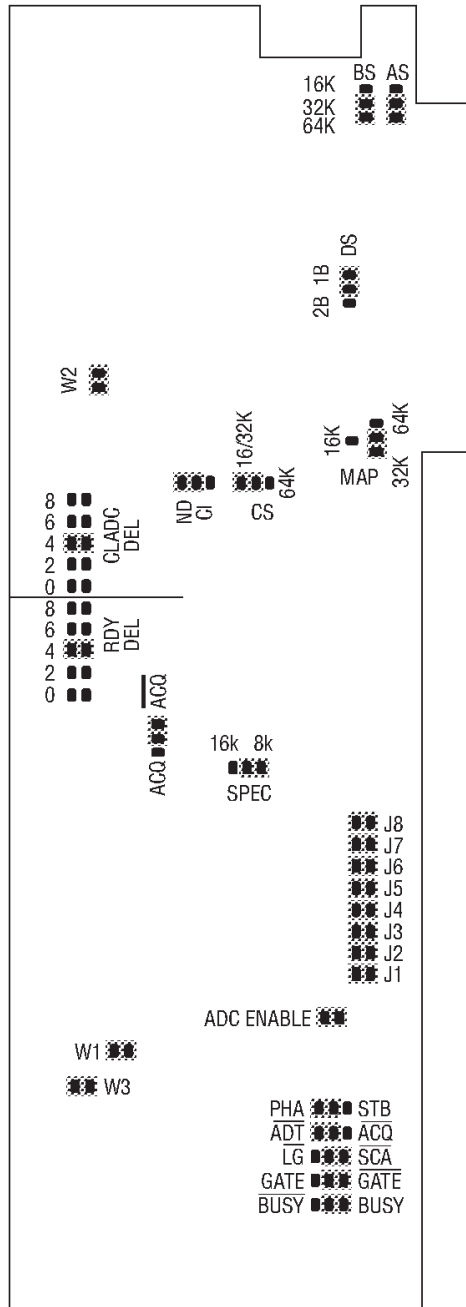


Figure 40 AccuSpec A and NaI Jumper Positions

Table 4 AccuSpec A and NaI Address Settings

ADC No.:	1	2	3	4
I/O Addr	300	310	320	330
Switch: A10	CLOSED	CLOSED	CLOSED	CLOSED
A9	OPEN	OPEN	OPEN	OPEN
A8	OPEN	OPEN	OPEN	OPEN
A7	CLOSED	CLOSED	CLOSED	CLOSED
A6	CLOSED	CLOSED	CLOSED	CLOSED
A5	CLOSED	CLOSED	OPEN	OPEN
A4	CLOSED	OPEN	CLOSED	OPEN

### LFC Enable Switches

Must always be in the “CLOSED” or “ON” position. The Model 599 LFC module cannot be used with the AccuSpec/A or /NaI ADC.

### ADC Interface Transfer Times

RDY DEL and CLADC DEL jumpers should be in position “4”.

### Memory Window Mapping.

There are five jumpers used to select the memory size, window size, and window location. The normal settings are:

AS=32/64K  
 BS=32/64K  
 CS=16/32K  
 DS=1B  
 MAP = 32K.

Other positions for these jumpers are not used by the Genie-2000 software.

### Spectrum Size

Leave jumper in the 8K position.

### **ADC Enable**

Leave installed, enabling on-board ADC.

### **MUX Selection Jumpers**

Remove all eight jumpers J1 through J8 when using a Model 589 or Model 8224 Analog Multiplexer; otherwise J1 through J8 should be left installed.

### **External Strobe Selection**

Leave the jumper in the “PHA” mode for normal (discriminator-triggered) PHA operation. Place the jumper in the “STB” position for externally gated conversions. With a Model 589 or Model 8224 Analog Multiplexer, the jumper must be in the STB position.

### **External Signal Selection**

There are four jumpers to select external signal and polarities. The normal settings are “BUSY”, “GATE\*”, “SCA\*”, and “ADT\*”. The optional positions are explained in the external signal descriptions of Appendix D, *Technical Information*.

### **Interface Signal Selection**

Leave jumpers in “ND” and “ACQ\*” positions.

### **W1, W2 and W3**

W1, W2, and W3 are manufacturing test jumpers; they must be left installed.

## **AccuSpec B**

Specific jumpering instructions for AccuSpec B boards are given in Figure 41 and Table 5.

### **Base I/O Address Switches**

The address switches should be set to (hexadecimal) 300, 310, 320 and 330 for units 1, 2, 3 and 4, respectively, unless other hardware interferes. The switches are labeled A4 through A10. An OFF or OPEN switch is a 1. An ON or CLOSED switch is a 0.

Switch settings for the four standard addresses are shown in Table 5.

### **LFC Enable Switches**

Place in the “CLOSED” or “ON” position for normal PHA acquisition. Place in the “OPEN” or “OFF” position to enable LFC acquisition when connected to a Model 599 LFC module.

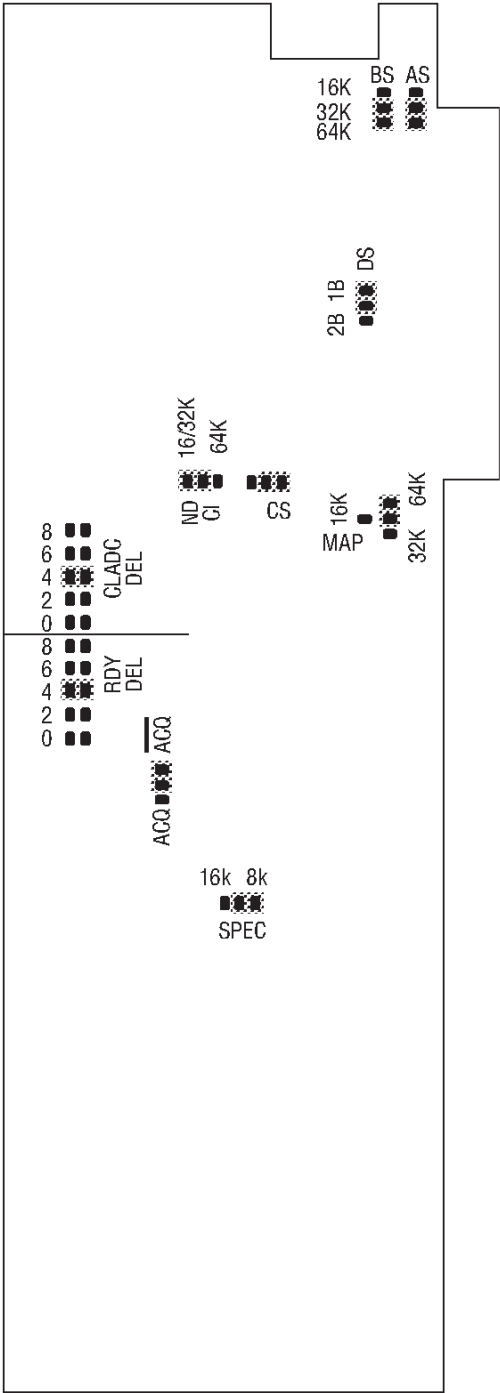


Figure 41 AccuSpec B Jumper Positions



Table 5 AccuSpec B Address Settings

Board No.:	1	2	3	4
I/O Addr Switch:	300	310	320	330
A10	CLOSED	CLOSED	CLOSED	CLOSED
A9	OPEN	OPEN	OPEN	OPEN
A8	OPEN	OPEN	OPEN	OPEN
A7	CLOSED	CLOSED	CLOSED	CLOSED
A6	CLOSED	CLOSED	CLOSED	CLOSED
A5	CLOSED	CLOSED	OPEN	OPEN
A4	CLOSED	OPEN	CLOSED	OPEN

### ADC Interface Transfer Times

The board is shipped with both the RDY DEL and CLADC DEL jumpers in position “4” (1.0  $\mu$ s delay and transfer times). Longer times may be selected with position “6” (1.5  $\mu$ s) or position “8” (2.0  $\mu$ s) when long ADC cables are used; shorter times may be selected with position “2” (0.5  $\mu$ s) when short cables and fast ADCs are used.

### Memory Window Mapping

There are five jumpers used to select the memory size, window size, and window location. The normal settings are:

AS=32/64K  
 BS=32/64K  
 CS=64K  
 DS=1B  
 MAP = 64K

Other positions for these jumpers are not used by the Genie-2000 software.

### Spectrum Size

The SPEC jumper is placed in the “16K” position when a 16K ADC is used. The SPEC jumper must be in the “8K” position if an older 8K ADC is used or if 2 groups of 8K are to be used.

### **Interface Signal Selection**

Jumpers are normally in “ND” and “ACQ” position for use of the interface with a Canberra ADC.

### **W2**

W2 is a manufacturing test jumper; it must be left installed.

## **AccuSpec NaI Plus**

Specific jumpering instructions for AccuSpec NaI Plus boards are given in Figure 42 and Table 6.

### **Base I/O Address Switches**

The address switches should be set to (hexadecimal) 300, 310, 320 and 330 for units 1, 2, 3 and 4, respectively, unless other hardware interferes. The switches are labeled A4 through A10. An OFF or OPEN switch is a 1. An ON or CLOSED switch is a 0.

Switch settings for the four standard addresses are shown in Table 6.

### **Memory Window Mapping**

A jumper in position “16LO” (actually a trace) places the 16K byte memory at a 32K address boundary (for instance, D0000 or D8000).

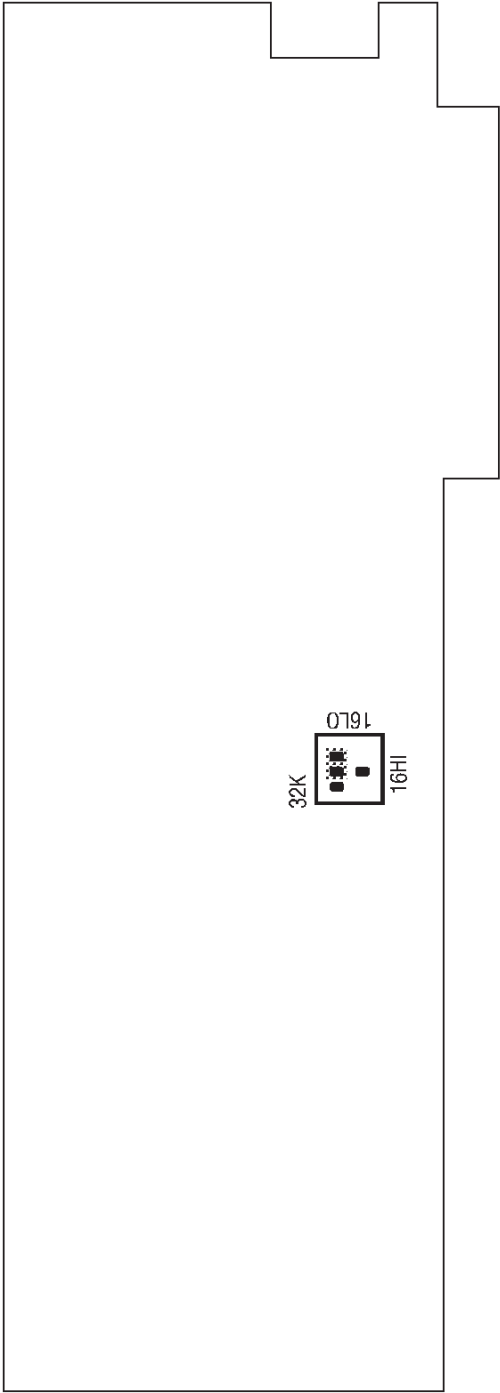


Figure 42 AccuSpec NaI Plus Jumper Positions

Table 6 AccuSpec Nal Plus Address Settings

Board No.:	1	2	3	4
I/O Addr Switch:	300	310	320	330
A10	CLOSED	CLOSED	CLOSED	CLOSED
A9	OPEN	OPEN	OPEN	OPEN
A8	OPEN	OPEN	OPEN	OPEN
A7	CLOSED	CLOSED	CLOSED	CLOSED
A6	CLOSED	CLOSED	CLOSED	CLOSED
A5	CLOSED	CLOSED	OPEN	OPEN
A4	CLOSED	OPEN	CLOSED	OPEN

## AccuSpec FMS

Specific jumpering instructions for AccuSpec FMS boards are given in Table 7.

### Base I/O Address Switches

The address switches should be set to (hexadecimal) 300, 310, 320 and 330 for units 1, 2, 3 and 4, respectively, unless other hardware interferes. The switches are labeled A4 through A10. An OFF or OPEN switch is a 1. An ON or CLOSED switch is a 0.

Switch settings for the four standard addresses are shown in Table 7.

### Memory Window Mapping

A jumper (labeled MAP) places the 16K byte memory at either a 64K or 32K address boundary (for instance, D0000 or D8000).

Table 7 AccuSpec FMS Address Settings

Board No.:	1	2	3	4
I/O Addr Switch:	300	310	320	330
A10	CLOSED	CLOSED	CLOSED	CLOSED
A9	OPEN	OPEN	OPEN	OPEN
A8	OPEN	OPEN	OPEN	OPEN
A7	CLOSED	CLOSED	CLOSED	CLOSED
A6	CLOSED	CLOSED	CLOSED	CLOSED
A5	CLOSED	CLOSED	OPEN	OPEN
A4	CLOSED	OPEN	CLOSED	OPEN

### Installing the Boards

Refer to your computer's operating manual for instructions on installing option cards (also called adapters). Each AccuSpec board requires a full-length option slot. In addition, use of an AccuSpec A or NaI with an analog multiplexer requires an extra rear-panel opening for the multiplexer connector.

If you have a hard disk mounted on a plug-in adapter card, you may need to put the AccuSpec A, NaI and NaI Plus boards as far as possible from the disk drive, as magnetic fields from the drive motor may introduce noise which degrades the usable resolution of the ADC. AccuSpec B boards may be placed anywhere that space allows.

Ensure that you have the required number of slots available for the boards in the computer or in an expansion chassis. To install your board(s):

**CAUTION** Turn off your computer. Never insert or remove any adapter board when the computer is on; severe damage to your computer or adapter may result.

1. Loosen the screws and gently remove the system's cover.

2. Remove the expansion slot cover by loosening the screw on the rear of the selected expansion slot lifting it up.
3. Place the AccuSpec board in an available expansion slot.
5. Insert the adapter(s) into the expansion slot(s) and firmly press it into place until the board clicks. Replace and tighten the screw.
6. Replace the system cover.
7. Your board is installed. Now you must configure your system to recognize the board. See Chapter 2, *MCA Input Definition Editor*.

## Other Hardware

If there is any other hardware, such as adapters or memory, to be installed, follow the instructions included with each item.

## Peripherals

Windows provides for hard copy to printers and plotters using the computer's serial (COMn) and Parallel (LPTn) interfaces. Before replacing the cover, note what interfaces are installed, their addresses (for instance, COM1 or COM2), and slot locations; you'll need this information when you connect the peripheral's cable.

## Display Adapters

Though Windows will operate with a wide variety of Display Adapters, Genie-2000 software is optimized for the SVGA display. Note which subsystem you are using; it will be needed in the Windows installation.

Reconnect the cables that were removed earlier, then turn the power ON and verify that the Power On System Test passes.

Turn power OFF and reinstall the cover. Before installing the system unit cover, make sure to check your computer manuals. Some models may require moving internal switches.

## Memory

Windows and the Genie-2000 software require a minimum of eight Megabytes of RAM, but will have greatly improved performance with more memory. For better sys-

tem performance, Canberra recommends you use memory that plugs directly into the motherboard instead of memory boards that plug into the system bus.

## Connecting the System

This section describes a typical Genie-2000 system. Refer to Figure 43.

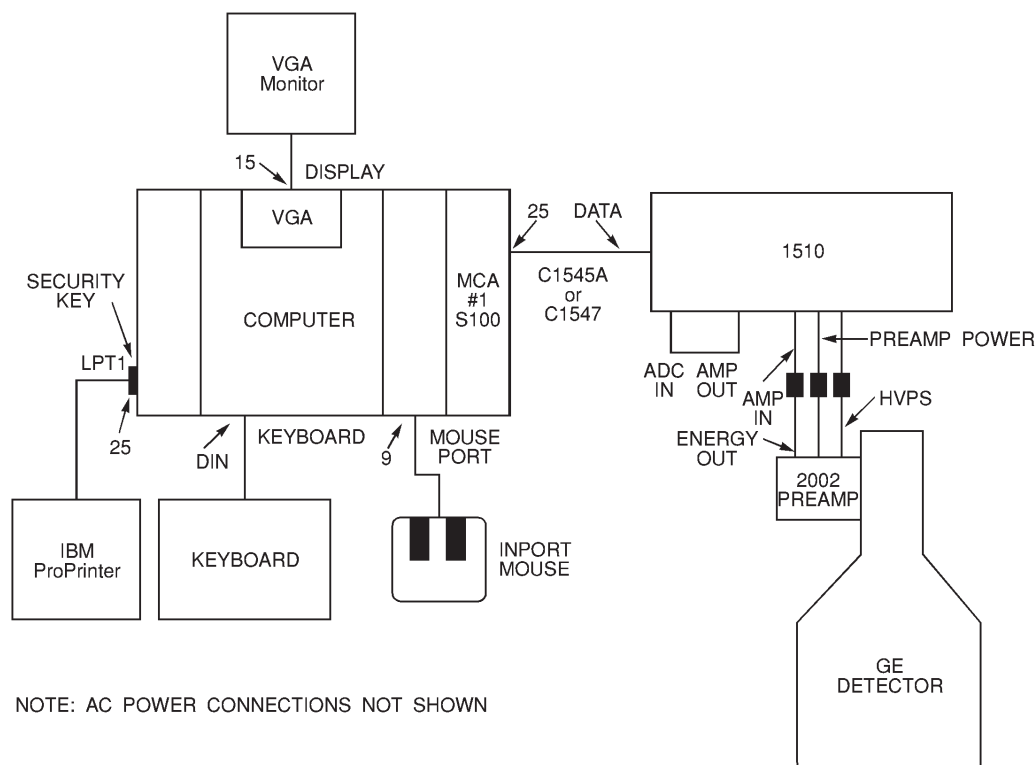


Figure 43 Typical System Configuration

- IBM 386-based computer, or compatible
- VGA display card and monitor
- Genie-2000 security key
- Microsoft InPort Mouse
- IBM ProPrinter
- Canberra Model 4610 Master MCA Board

- Canberra Model 1510 Integrated Signal Processor (or equivalent NIM modules and NIM Bin)
  - Canberra Germanium Detector
  - Radioisotope Source
1. Connect the keyboard to the DIN connector on the lower part of the computer's rear panel.
  2. Connect the Microsoft InPort Mouse to the mouse port on the rear panel.
  3. Connect the VGA display's 15-pin video cable to the Display connector.
  4. Connect the Genie-2000 security key to any available parallel port.
  5. Connect the C-1548 cable, or equivalent, between the printer and LPT1.
  6. Connect the 1510's DATA connector to the MCA board with the supplied C1547 cable.

The optional C-1545A 3 m shielded ribbon cable has a black wire with a ring lug on the ADC end, which is to be grounded on a grounding screw on the ADC's rear panel. The black wire at the computer end of the cable must be retained between the threaded insert on the rear panel and the metal shell on the cable connector.

Note: To avoid inducing resolution degrading noise into the signal cables, route the coaxial cables away from the Display Monitor.

7. Connect the 1510's ADC IN to its AMP OUT with the 15 cm BNC to BNC coax cable supplied with the 1510.
8. Connect the Preamp's ENERGY output to the 1510's AMP IN cable with another BNC to BNC coax cable.
9. Connect the detector's PREAMP POWER cable to the 1510 with the supplied A22541 Preamp Power Extender Cable.
10. Connect the 1510's HVPS OUT connector to the Preamp with the supplied coax cable with SHV connectors at each end. Check the polarity and operating voltage requirements of the detector before turning on the HVPS.



## Installing an 8223 or 8224 Multiplexer

Genie-2000 Software supports multiple input systems with the Model 8224 Analog Multiplexer through six of our current MCA hardware systems.

- Model 556 AIM, when used with an 8700 NIM ADC.
- AccuSpec A Board, with an on-board ADC.
- AccuSpec NAI Board, with an on-board ADC.
- AccuSpec B Board, when used with an 8700 NIM ADC.
- System 100 Board, when used with an 8700 NIM ADC.

Note Genie-2000 software does not currently support Group Start/Stop control of the 8224. This means that the accessories for Independent Start/Stop control must be purchased in order to use the 8224 with Genie-2000 and any of these MCA products.

Table 8 summarizes the supported multiplexer configurations and their capabilities for the above MCA hardware systems.

Table 8 Genie-2000 Software vs. ADC and Multiplexer

<b>MCA Hardware</b>	<b>ADC</b>	<b>8223 Group Start/Stop</b>	<b>8224 Group Start/Stop</b>	<b>8224 Independent Start/Stop</b>
AIM	Any 8700 ADC	Not functional	Not functional	16 inputs
AccuSpec A AccuSpec NaI	On board	Not functional	Not functional	8 inputs

## **Genie-2000/AIM/8700 ADC Systems**

Genie 2000 can be used in conjunction with a 556 AIM, a 554 RPI, 8700 ADCs and 8244 AMXs for multiplexer systems with Independent Start/Stop Control.

### **A 16-Input System**

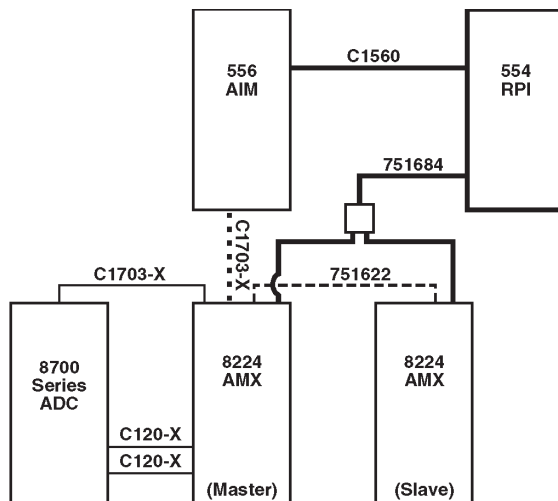
The MCA/ADC system shown in Figure 44 supports up to two Model 8224 AMXs for a maximum of 16 inputs with Independent Start/Stop Control.

Note: The Independent Start/Stop control accessories described in Figure 44 are not optional. Independent Start/Stop Control is required when using 8224's.

### **A 32-Input System**

A 16-input system can be expanded to 32 inputs by connecting a second ADC with its two 8224s to the AIM's ADC 2 input in the system shown in Figure 44.

Though a single AIM is limited to two ADCs and 32 inputs, a larger system can be assembled, using a second AIM.



- ADC-AMX Connections**  
 Each 8224 AMX is supplied with one C1703-2 Interface Cable.  
 The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.
- AIM-AMX Connection**  
 Each AIM is supplied with two C1703-2 Interface Cables.
- AMX Master-Slave Connection**  
 Each slave requires a 751622 Expansion Cable that must be purchased separately.
- Independent Start/Stop for the 8224 AMXs**  
 Requires the purchase of a Model 554 Remote Parallel Interface (RPI) and at least one 751684 cable assemblies. Each 751684 Cable Assembly supports two 8224s and each RPI supports 2 such cable assemblies. The 751839 ICB cable to connect the RPI to the AIM is supplied with the AIM.  
 Independent Start/Stop Control can also be accomplished for a single 8224 with the 751776 Control Cable and a parallel port (LPT), but this is not recommended when using an AIM.

Figure 44 8224 Cabling for Genie 2000/AIM/8700 ADC

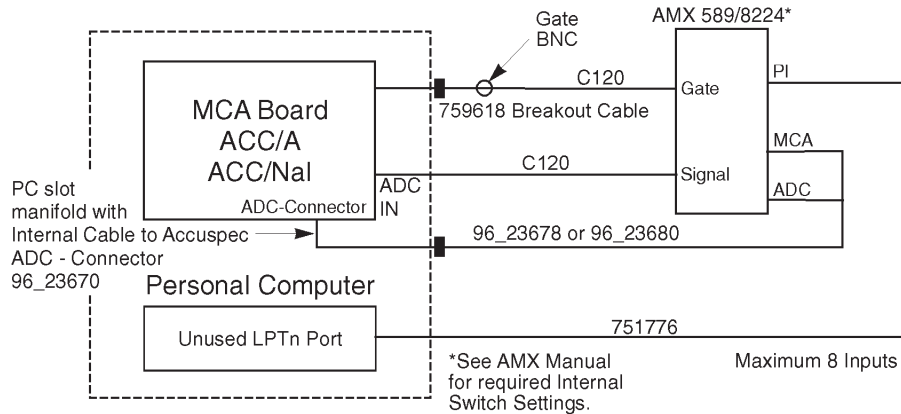
## Genie-2000/AccuSpec A or Nal Systems

Genie-2000 Software supports multiple input systems with both the AccuSpec A and NAI Board MCAs and the Model 8224 AMX. Genie-2000 support is limited to one 8224 per board and is only functional for Independent Start/Stop Control.

The AccuSpec A or NAI board's jumpers must be set for: STB,  $\overline{\text{ADT}}$ ,  $\overline{\text{SCA}}$ ,  $\overline{\text{GATE}}$ , BUSY, J1-J8 OUT and the LFC jumper in the CLOSED (disabled) position.

**Note** The configuration shown in Figure 45 requires a PC with two parallel ports (LPTs), one for the Genie-2000 security key and a second for Independent Start/Stop Control.

## Installing an 8223 or 8224 Multiplexer



**Accuspec A or NAI MCA and ADC Connections to the 8224 AMXs**  
 Require interface Kit 840617 or 840618 to be purchased. These kits contain the 96A\_23678 or 96A\_23680 external PCAl-AMX cable, the 759618 breakout cable for the Gate Connection, and the 96\_23670 PC slot manifold.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

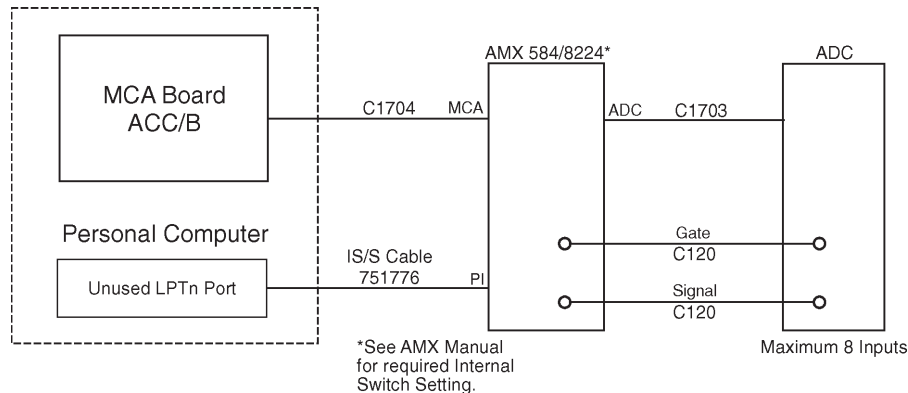
**Independent Start/Stop for the 8224 AMX**  
 Requires a free LPT and a 751776 Control Cable. The Cable must be purchased separately.

Figure 45 8224 Cabling with AccuSpec A or NaI

## Genie-2000/AccuSpec B/8700 ADC Systems

Genie-2000 Software supports multiple input systems with the AccuSpec B Board MCAs and the Model 8224 AMX. Genie-2000 support is limited to one 8224 per board and is only functional for Independent Start/Stop Control. The AccuSpec B board's LFC jumper must be in the CLOSED (disabled) position.

**Note** The configurations shown in Figure 46 require a PC with two parallel ports (LPTs), one for the Genie-2000 security key and a second for Independent Start/Stop Control.



**ADC-AMX Connections**

Each 8224 AMX is supplied with one C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

**Accuspec B or MC Board to AMX Connection**

Each Accuspec B or MC Board is supplied with one C1704-10 Interface Cable.

**Independent Start/Stop for the 8224 AMX**

Requires a parallel port (LPT) and a 751776 Control Cable. The Cable must be purchased separately.

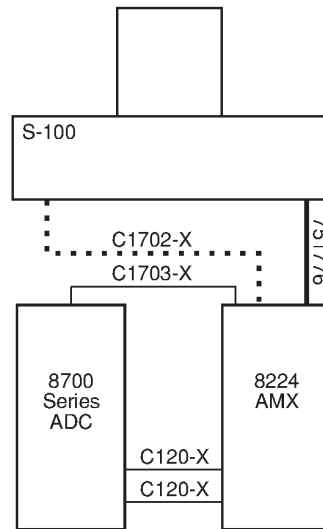
Figure 46 8224 Cabling for AccuSpec B

## Genie-2000/System 100/8700 ADC Systems

Genie-2000 Software supports the use of the 8224 AMX with the System 100 Board MCA and any 8700 Series ADC. Genie-2000 support is limited to one 8224 per system and is only functional for Independent Start/Stop Control.

If you need more than eight inputs with the Genie-2000 System 100 configuration, you'll have to use the 1520 Integrated Signal Processor instead of the 8224 and an 8700 Series ADC. Genie-2000 support for the 1520 is also limited to the Independent Start/Stop Control Mode.

**Note** The configuration shown in Figure 47 requires a PC with two parallel ports (LPTs), one for the Genie-2000 security key and a second for Independent Start/Stop Control.



- **ADC-AMX Connections**  
 Each 8224 AMX is supplied with a C1703-2 Interface Cable.  
 The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.
- ..... **System 100 Board to 8224 AMX Connection**  
 Each System 100 Board is supplied with a C1702-4 Interface Cable.
- **Independent Start/Stop for the 8224 AMX**  
 Requires a parallel port (LPT) and a 751776 Control Cable.  
 The Cable must be purchased separately.

Figure 47 Cabling with System 100 and 8700 ADC

## Multi-Channel Scaling Experiments

If you are using a Model 8082 MCS Unit, it can be substituted for the ADC. Note the following:

1. The 8082 requires a +6 V supply from its NIM Bin (Model 2100 or equivalent).
2. If you're using the normal 1.2 m cable, the "ear-type" cable latches must be removed.
3. Cables C-1545A, C1545B and C1550A are available. These optional 3 m shielded cables connect the MCA board to the 25-pin data and 9-pin control connectors on the module. The shield leads must be grounded at the MCS unit. One of the screws in the side cover makes a convenient ground point. The black wire at the computer end must be retained between the threaded insert on the rear panel and the metal shell on the cable connector.

## Sample Changer Control

With a System 100 MCA, a sample changer control output is provided by the board. For sample changer control with an AIM MCA, refer to the Model 556 AIM and Model 554 RPI User's Manuals. Figure 48 shows the sample changer signals timing diagram.

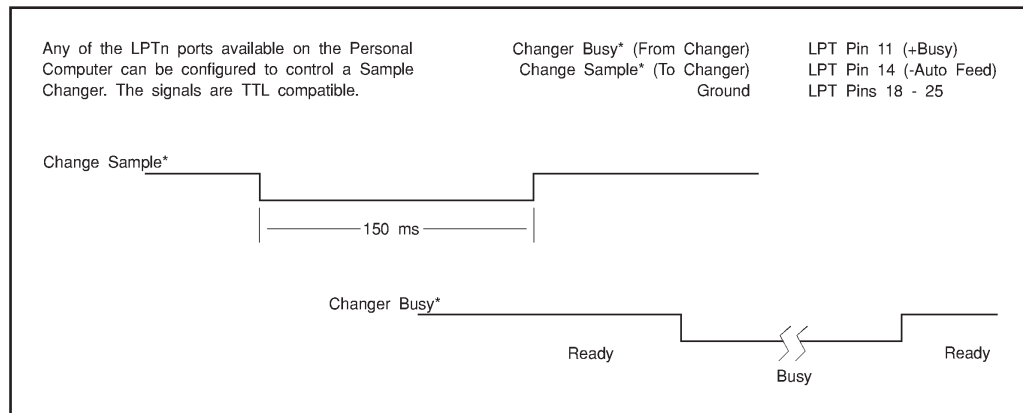


Figure 48 Sample Changer Timing Diagram

## LPT Parallel Port Assignments

In order to control a sample changer or an AMX module through an LPT (parallel) port, the port must be assigned to the device to be controlled (refer to “Address Settings” on page ). In order to know which LPT port number to use, you must know which physical address is assigned to which logical port number.

Refer to your computer's technical documentation or use the Windows Control Panel's System icon to determine which physical parallel ports are available and what address has been assigned to each one.

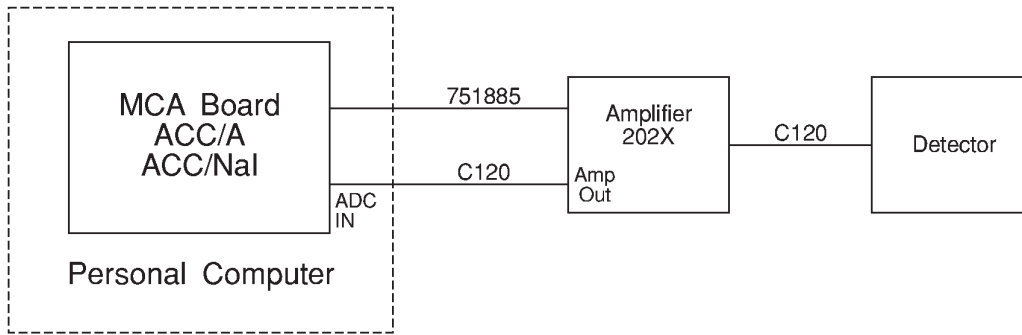
## AccuSpec Setup Diagrams

These diagrams are included to help you set up your AccuSpec system. The board jumper positions for each of the systems are shown in the following table.

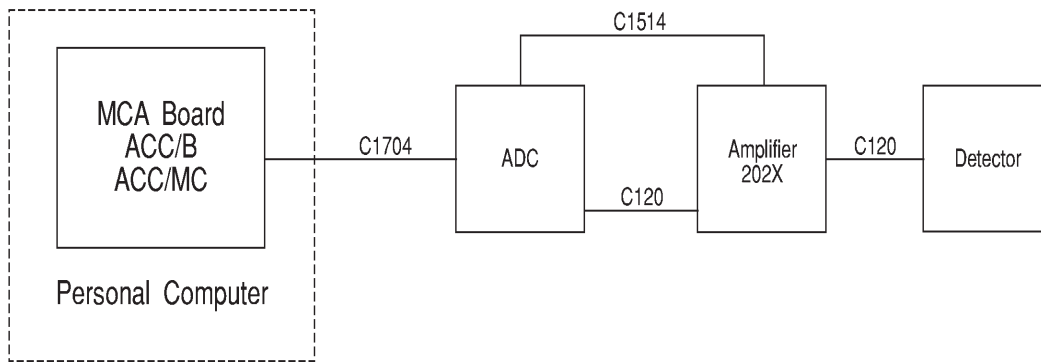
<b>System</b>	<b>MCA Board</b>						
A	AccuSpec A/NaI	PHA	$\overline{\text{ADT}}$	$\overline{\text{LG}}$	$\overline{\text{GATE}}$	$\overline{\text{BUSY}}$	J1-J8 IN
B	AccuSpec B/MC	–	–	–	–	–	–
C	AccuSpec B/MC	–	–	–	–	–	–
<b>System</b>	<b>LFC Switch</b>						
A	CLOSED (disabled)						
B	CLOSED (disabled)						
C	OPEN (enabled)						
<b>System</b>	<b>Amplifier</b>						
A	ALL	DT	Output to ADC				
B	ALL	DT	Output to ADC				
C	Except 2020	BSY	Output to ADC				



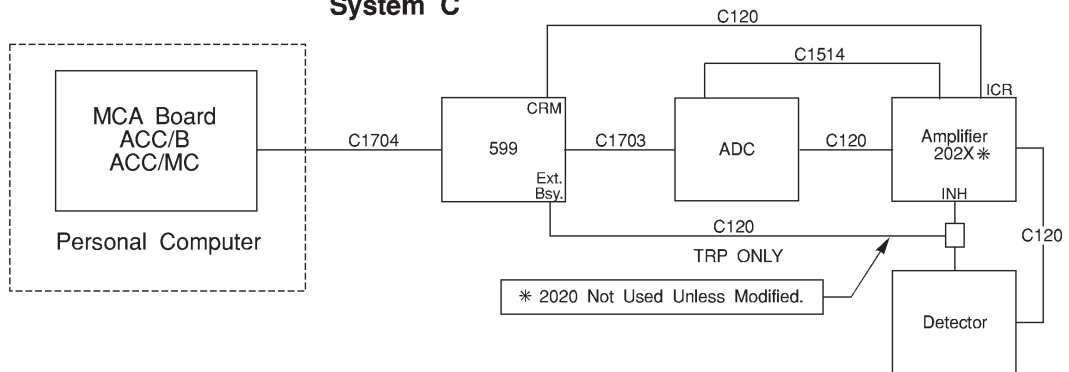
### System A



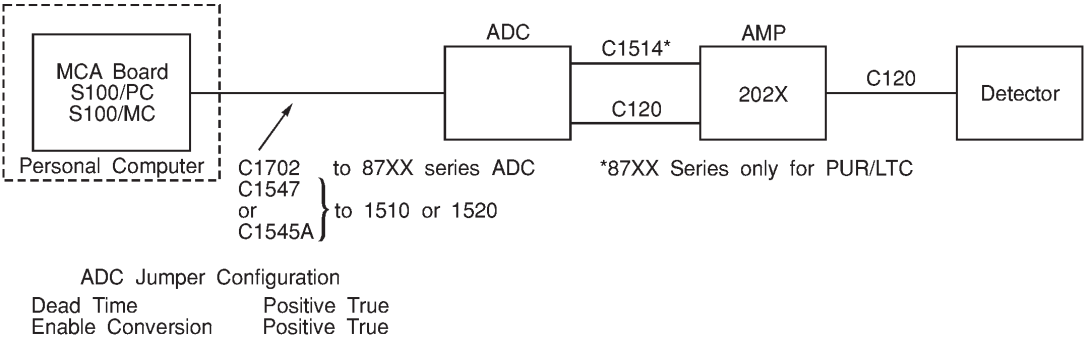
### System B



### System C



# System 100 Setup Diagram



## 4. Technical Information

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This appendix covers the specifications of Genie-2000's System 100 and AccuSpec hardware and includes troubleshooting tips. AIM hardware information will be found in the AIM User's Manual and ICB NIM hardware information in the AIM/ICB System Installation Manual.

For consistency, all negative true signals are followed by a slash (SIGNAL/). Note, however, that on all AccuSpec schematics negative true signals are shown by a following asterisk (SIGNAL\*).

### System 100 MCA Boards

The System 100 MCA boards are standalone microprocessor based sub-systems. Commands from the Host computer are sent to the boards for execution. These commands include:

- Acquire Start
- Acquire Stop (The board looks for presets, but Host can stop if operator does an Acquire Stop.)
- Clear
- Read out/Read in Data
- Read out Scaled Data for Display
- Read out Calculated ROI Data (Integral, Area, % Error, etc.)
- Clear Timers/Sweep Counter
- Abort Command

All communication with the board is done using INput and OUTput commands on the 8-bit computer (PC or Micro Channel) bus. Single word commands cause an NMI interrupt to the MCA processor. Multi-word commands and all data transfer to the Host is done through the on-chip DMA controller between the computer bus and on-board dynamic RAM. The MCA program resides in EPROM.

The System 100 may be configured with up to four plug-in multichannel analyzer boards. Each board includes its own 16-bit microprocessor and 16-bit on-board data paths. Sufficient RAM, ROM and logic is included to enable the MCA/Memory board

to operate as a standalone high performance 16K-channel MCA for data acquisition, storage, and display buffering.

## System 100 ISA Specs

Specifications for the ISA Bus MCA Boards.

### MCA/Memory

#### Processor

Intel 80186 16-bit microprocessor, 8 MHz, zero wait state RAM.

#### Memory

16 384 data channel memory,  $2^{32}-1$  counts per channel. Configurable as 16 384, 8192, or 4096 channel full memory, divisible into halves, quarters, eighths and sixteenths.

#### Storage Modes

PHA and MCS, choice of Add or Subtract

#### Presets

PHA: Live Time or True Time, from 1 to  $10^7-1$  seconds in 1.0 second increments; counts in a range of channels; and gross integral or net area of a Region of Interest.

MCS: Number of sweeps, from 1 to  $10^9-1$ .

#### Display Formatting

Maximum of 1024 points with 11-bit resolution per data channel.

### Collect Interface

Type: Direct Memory Access (DMA) to an on-board, dual port 16 384 channel data memory.

PHA: Compatible with all Canberra ADCs.

Mixer/Router: System 100 expandable to 16 PHA inputs using the Model 1520 Integrated ADC-Mixer/Router and Model 4622 Control Interface. Individual inputs on the 1520 Mixer/Router will have an independent Live Time or True Time preset. For eight PHA inputs, a Model 8224 AMX with a 75-1776 Control Cable can be used.

MCS: Compatible with Canberra Model 8082 NIM MCS Unit.

Cycle Time: Less than 3  $\mu$ s (average)

### Sample Changer

TTL Outputs: Sample Advance and Acquire Status.

TTL Inputs: Changer Ready and Acquire Stop.

### Host Bus Interface

Type – 8-bit PC Bus Interface, I/O mapped, Program Polling Interface (no interrupt).

### I/O Address

Primary Range – 340<sub>H</sub> through 35D<sub>H</sub>. Alternate Range – 300<sub>H</sub> through 31D<sub>H</sub>

### Power

+5 V, 1.3 A, nominal

-12 V, 0.5 mA

### Self Test

Power on check of PROM, RAM, DMA channels, and Timer.

### Physical

Size: 33.53 x 10.67 cm (13.2 x 4.2 in.) length x height

Weight: 340 gm (12 oz)

Rear Panel: J101 – 25-pin female D style for ADC/MCS Interface. J102 – 9-pin female D style for Remote Control

Internal Controls:

Board Number (2).

Alternate Address Select (1).

Bus Ready Select (2).

PROM/EPROM/RAM Select (3).

Expansion Connectors: Two 34-pin ribbon headers.

See Figure 55 on page 101 for jumper locations.

### Internal Controls

W1 Prom Select

1 to 2 – 64K or 128K

2 to 3\* – 256K

W2 SRAM/EEPROM/PROM Select

1 to 2 – SRAM/EEPROM

2 to 3\* – PROM

W3 Prom Select

1 to 2\* – K (64K, 128K, 256K)  
2 to 3 – 512 K

W5 Ready Select Decode

1 to 2\* – Port 2  
2 to 3 – Port 3 Read

W7 Ready Select Output

1 to 2 – SDO  
2 to 3\* – I/O CH RDY

\*Factory default, all boards

**Board Select Jumpers**

W6 MB Code

1 to 2 – MB  
2 to 3 – NOT MB

W8 MA Code

1 to 2 – MA  
2 to 3 – NOT MA

MCA#	W6	W8
1 <sup>1</sup>	2 to 3	2 to 3
2 <sup>2</sup>	2 to 3	1 to 2
3 <sup>1</sup>	2 to 3	2 to 3
4 <sup>1</sup>	2 to 3	1 to 2

W9 PC Address Select

1 to 2 – Alternate  
2 to 3<sup>3</sup> – Primary

<sup>1</sup>Factory Default, Model 4610

<sup>2</sup>Factory Default, Model 4611

<sup>3</sup>Factory Default, All Boards

**Input/Output**

This is a brief overview of the PC bus MCA's two I/O connectors, J101 and J102 (J103 is a connector for automated test equipment). For more detailed information, re-

fer to the J101 Connector description on page 74 or the J102 Connector description on page 77.

**J101 – ADC/MCS**

<u>Function</u>	<u>Direction</u>	<u>TTL Polarity</u>
14 Address Lines	In/Out <sup>4</sup>	L
Data Ready	In	L
Data Invalid	In	L
Inhibit Add One	In	L
Dead Time	In	H
Enable Data	Out	L
Enable Converter	Out	H
Data Accepted	Out	L
MCS Mode	Out	L
I/O CMD <sup>4</sup>	Out	L
I/O ACK <sup>4</sup>	In	L

4. With the optional Model 4612. Address lines are made bidirectional.

**J102 – Remote Control**

Changer Ready	In	H
Abort Collect	In	L
MCS End of Sweep	In	H
Changer Advance	Out	L
Collect Status	Out	L

**Rear Panel Connectors**

**J101 ADC/MCS Data Connector**

25-pin female D-connector with threaded inserts. ADC Timing is shown in Figure 49.

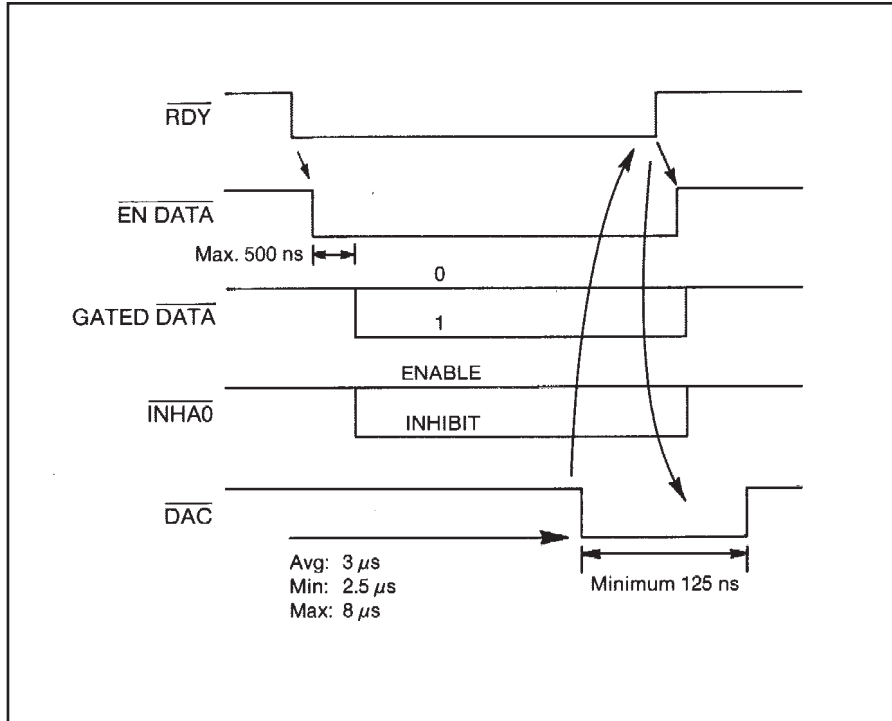


Figure 49 J101 Timing During ADC Storage

Unless otherwise stated, the Data Signal parameters are:

Inputs: Positive = 2.4 V to 5.0 V.  
 Negative = 0.0 V to 0.3 V.

Outputs: Positive = 2.4 to 5 V (0.4 mA at 2.4 V).  
 Negative = 0.0 to 0.5 V at 2 mA.

<u>Pin</u>	<u>Signal</u>	<u>In/Out</u>
1	2 <sup>0</sup> /	IN <sup>5</sup>
2	2 <sup>1</sup> /	IN <sup>5</sup>
3	2 <sup>2</sup> /	IN
4	2 <sup>3</sup> /	IN <sup>5</sup>
5	2 <sup>4</sup> /	IN <sup>5</sup>
6	2 <sup>5</sup> /	IN <sup>5</sup>
7	2 <sup>6</sup> /	IN <sup>5</sup>
8	2 <sup>7</sup> /	IN <sup>5</sup>
9	2 <sup>8</sup> /	IN <sup>5</sup>



## Technical Information

10	2 <sup>9</sup> /	IN <sup>5</sup>
11	2 <sup>10</sup> /	IN <sup>5</sup>
12	2 <sup>11</sup> /	IN <sup>5</sup>
13	2 <sup>12</sup> /	IN <sup>5</sup>
15	2 <sup>13</sup> /	IN <sup>5</sup>

Gated binary address data from ADC or MCS module from TTL Tri-state drivers. Enabled by signal ENDATA. TTL negative true signal. With the exception of 2<sup>12</sup> and 2<sup>13</sup>, unused inputs must be at stable logic level during ENDATA.

5. With the optional Model 4612, the address lines are bidirectional. In the OUT mode, controls are transferred to the Model 1520 ADC-M/R.

14	RDY/	IN	ADC conversion complete
			TTL negative true signal. Stays True until DAC/ generated.
16	INHАО/	IN	Inhibit Add One
			TTL Negative true signal. Signal state while ENDATA is true determines if memory is incremented. The open input is pulled positive.
17	DAC/	OUT	Data Accepted
			TTL negative true signal. Generated at end of ADC/MCS cycle. Stays True until ADC RDY/ goes false.
18	ENC	OUT	Enable Converter
			TTL positive true signal. Drive: 2 mA at 2.4; 2 mA at 0.4 V
19	MCS/	OUT	Multiscale Enabled
			TTL Negative true signal.
20	INV/	IN	Invalid ADC Conversion
			TTL negative true signal. No function with standard 4610/4611.
21	DT	IN	Dead Time
			Controls PHA Live time gating. TTL positive true signal. $V_{in} > 2.4V$ at 0.4 mA, disables PHA Live Timer from counting. $V_{in} < 0.5 V$ , or open circuit, enables PHA Live Timer to count.
22	ENDATA/	OUT	Enable Address Data
			TTL negative true signal. Drive: 2 mA at 2.4 V; 2 mA at 0.4 V.

- 23            I/O ACK IN  
Optional; only with Model 4612. Enables I/O controls from Model 4612. TTL negative true signal.
- 24            Ground
- 25            I/O CDM OUT  
Optional; only with Model 4612. Request from Model 4612 to send control signal to Model 1520. TTL negative true signal.

**J102 Remote Control**

9-pin female D-connector with threaded inserts. Remote Control Timing is shown in Figure 50.

Unless otherwise stated, the Remote Control Signal parameters are:

Inputs: Positive = 2.4 V to 5.0 V.  
Negative = 0.0 V to 0.3 V at 1 mA.

Outputs: Positive = 2.4 to 5 V (0.4 mA at 2.4 V).  
Negative = 0.0 to 0.5 V at 2 mA.

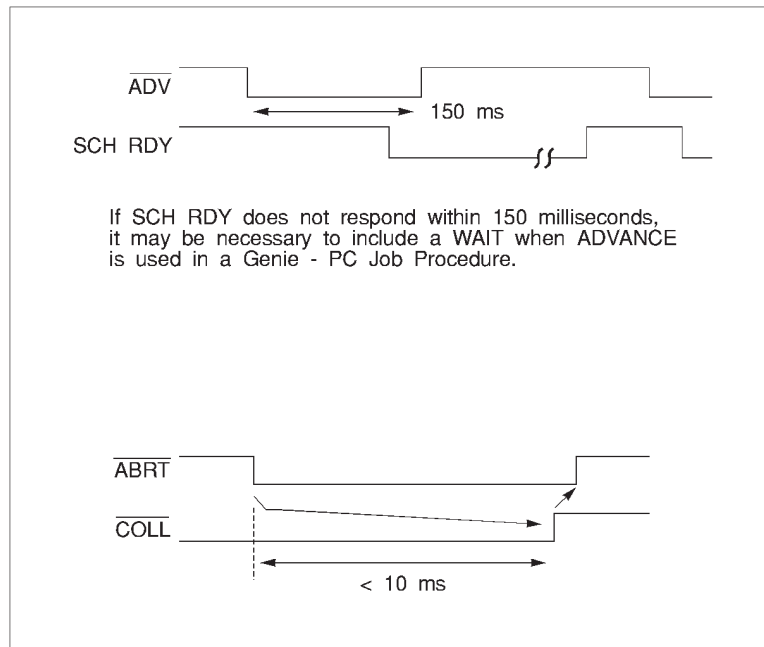


Figure 50 Remote Control Timing Diagram

## Technical Information

<u>Pin</u>	<u>Signal</u>	<u>In/Out</u>	<u>Description</u>
1	ABRT/	IN	Abort In TTL negative true signal. Ends Collect. Hold low until status changes (pin 4).
2	SCH RDY	IN	Sample Changer Ready In TTL positive true signal. If SCH RDY does not respond within 150 ms, it may be necessary to include a WAIT when ADVANCE is used in a Genie-2000 Job Procedure.
3	ADV/	OUT	Advance Out TTL negative true signal Approximate 150 ms pulse after command.
4	COLL/	OUT	Collect Status TTL negative true signal. True (low) when in Acquire Mode.
5	Ground		
6	Ground		
7	Ground		
8	AOF	IN	End of Sweep In TTL positive true signal. Used for MCS sweep counting. Minimum width 1 $\mu$ s.

### PC Host Bus Signals

SA0 through SA9. Latched Address lines used for I/O device decoding. TTL positive true. HCT buffers used for essentially zero dc loading.

SD0 through SD7. Data Bus bits 0 through 7 for byte transfer IN and OUT to Host. Gated onto bus during -IOR. TTL positive true.

Bus Loading: 20.0  $\mu$ A at 2.7 V; 0.2 mA at 0.4 V.

Bus Drive: 3.0 mA at 2.4 V; 24.0 mA at 0.5 V

AEN

Address Enable. When TTL low indicates that Host processor is controlling bus. HCT buffer used for essentially zero dc loading.

-IOR

I/O Read Signal. TTL negative true. Signals board that Host is doing an Input instruction. HCT buffer for essentially zero dc loading.

**-IOW**

I/O Write Signal. TTL negative true. Signals board that Host is doing an OUTput instruction. HCT buffer for essentially zero dc loading.

**RESET DRV**

Reset Drive. TTL positive true. Initializes MCA board. HCT buffer for essentially zero dc loading.

**I/O CH RDY**

I/O Channel Ready Output from board during access to Port 2. TTL positive True. Driven from tri-state device.

Bus Drive: 2.6 mA at 2.4 V; 12.0 mA at 0.4 V

Bus Loading in Tri-State: 20  $\mu$ A at 2.4 V; 20  $\mu$ A at 0.4 V

+5 V dc. Power to board: 1.3 A, nominal.

-12 V dc. Bias voltage to board. 0.5 mA.

## **System 100 Micro Channel Specs**

Specifications for the Micro Channel Bus MCA Board.

### **MCA/Memory**

#### **Processor**

Intel 80C186 16-bit microprocessor, 12 MHz, zero wait state RAM.

#### **Memory**

16 384 data channel memory,  $2^{32}$ -1 counts per channel. Configurable as 16 384, 8192, or 4096 channel full memory, divisible into halves, quarters, eighths and sixteenths.

#### **Storage Modes**

PHA and MCS, choice of Add or Subtract

#### **Presets**

PHA: Live Time or True Time, from 1 to  $10^7$ -1 seconds in 1.0 second increments; counts in a range of channels; and gross integral or net area of a Region of Interest.

MCS: Number of sweeps, from 1 to  $10^9$ -1.

#### **Display Formatting**

Maximum of 1024 points with 11-bit resolution per data channel.

### **Collect Interface**

Type: Direct Memory Access (DMA) to an on-board, dual port 16 384 channel data memory.

PHA: Compatible with all Canberra ADCs.

Mixer/Router: System 100 expandable to 16 PHA inputs using the Model 1520 Integrated ADC-Mixer/Router and Model 4612 Control Interface. Individual inputs on the 1520 Mixer/Router will have an independent Live Time or True Time preset. For eight PHA inputs, a Model 8224 AMX with a 75-1776 Control Cable can be used.

MCS: Compatible with Canberra Model 8082 NIM MCS Unit.

Cycle Time: Less than 3  $\mu$ s (average)

### **Sample Changer**

TTL Outputs: Sample Advance and Acquire Status.

TTL Inputs: Changer Ready and Acquire Stop.

### **Host Bus Interface**

Type – I/O mapped, Program Polling Interface (no interrupt).

### **I/O Address**

Primary Range – 340<sub>H</sub> through 35F<sub>H</sub>. Alternate Range – 300<sub>H</sub> through 31F<sub>H</sub>

### **Power**

+5 V, 0.8 A, nominal  
-12 V, 0.5 mA

### **Self Test**

Power on check of PROM, RAM, DMA channels, and Timer.

### **Physical**

Size: 29.2 x 8.83 cm (11.5 x 3.475 in.) length x height

Weight: 255 gm (9 oz)

Rear Panel: J101 – 25-pin female D style for ADC/MCS Interface. J102 – 8-pin female DIN style for Remote Control

Expansion Connectors: Two 34-pin ribbon headers.

**Input/Output**

This is a brief overview of the Micro Channel bus MCA's two I/O connectors, J101 and J102 (J103 is a connector for automated test equipment). For more detailed information, refer to the J101 Connector description on page 82 or the J102 Connector description on page 84.

**J101 – ADC/MCS**

<u>Function</u>	<u>Direction</u>	<u>TTL Polarity</u>
14 Address Lines	In/Out <sup>6</sup>	L
Data Ready	In	L
Data Invalid	In	L
Inhibit Add One	In	L
Dead Time	In	H
Enable Data	Out	L
Enable Converter	Out	L
Data Accepted	Out	L
MCS Mode	Out	L
I/O CMD <sup>6</sup>	Out	L
I/O ACK <sup>6</sup>	In	L

<sup>6</sup>With the optional Model 4622. Address lines are made bidirectional.

**J102 – Remote Control**

Changer	ReadyIn	H
Abort Collect	In	L
MCS End of Sweep	In	H
Changer Advance	Out	L
Collect Status	Out	L
Reset	In	L

**Rear Panel Connectors**  
**J101 ADC/MCS Data Connector**

25-pin female D-connector with threaded inserts. ADC Timing is shown in Figure 51.

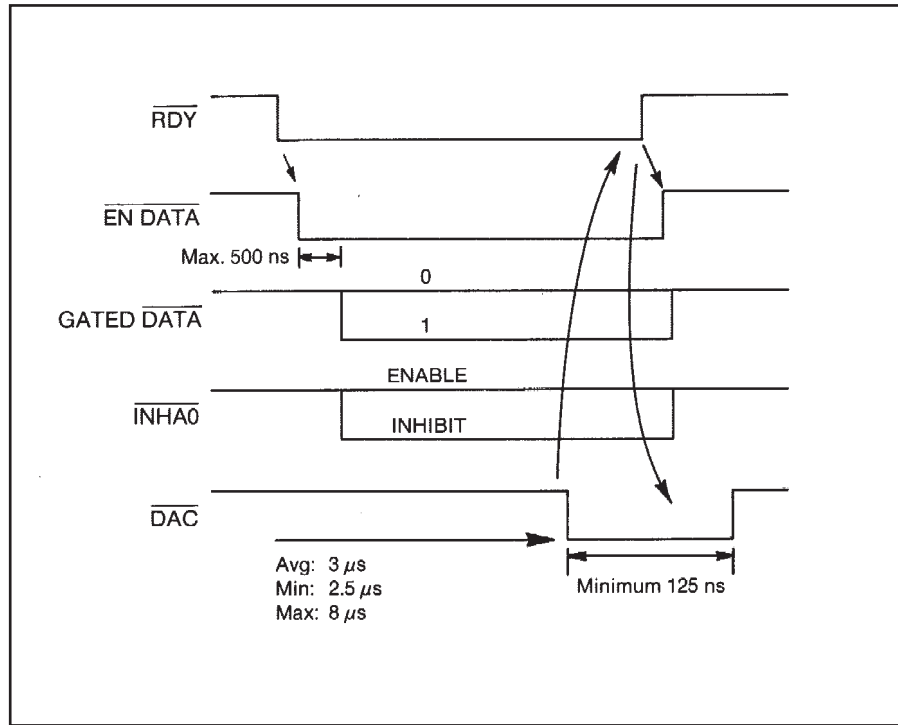


Figure 51 J101 Timing During ADC Storage

Unless otherwise stated, the Data Signal parameters are:

Inputs: Positive = 2.4 V to 5.0 V.  
 Negative = 0.0 V to 0.3 V.

Outputs: Positive = 2.4 to 5 V (0.4 mA at 2.4 V).  
 Negative = 0.0 to 0.5 V at 2 mA.

<u>Pin</u>	<u>Signal</u>	<u>In/Out</u>
1	2 <sup>0</sup> /	IN <sup>7</sup>
2	2 <sup>1</sup> /	IN <sup>7</sup>
3	2 <sup>2</sup> /	IN <sup>7</sup>

4	2 <sup>3</sup> /	IN <sup>7</sup>
5	2 <sup>4</sup> /	IN <sup>7</sup>
6	2 <sup>5</sup> /	IN <sup>7</sup>
7	2 <sup>6</sup> /	IN <sup>7</sup>
8	2 <sup>7</sup> /	IN <sup>7</sup>
9	2 <sup>8</sup> /	IN <sup>7</sup>
10	2 <sup>9</sup> /	IN <sup>7</sup>
11	2 <sup>10</sup> /	IN <sup>7</sup>
12	2 <sup>11</sup> /	IN <sup>7</sup>
13	2 <sup>12</sup> /	IN <sup>7</sup>
15	2 <sup>13</sup> /	IN <sup>7</sup>

Gated binary address data from ADC or MCS module from TTL Tri-state drivers. Enabled by signal ENDATA. TTL negative true signal. With the exception of 2<sup>12</sup> and 2<sup>13</sup>, unused inputs must be at stable logic level during ENDATA.

7. With the optional Model 4622, the address lines are bidirectional. In the OUT mode, controls are transferred to the Model 1520 ADC-M/R.

14	RDY/	IN	ADC conversion complete
			TTL negative true signal. Stays True until DAC/ generated.
16	INHAO/	IN	Inhibit Add One
			TTL Negative true signal. Signal state while ENDATA is true determines if memory is incremented. The open input is pulled positive.
17	DAC/	OUT	Data Accepted
			TTL negative true signal. Generated at end of ADC/MCS cycle. Stays True until ADC RDY/ goes false.
18	ENC	OUT	Enable Converter
			TTL positive true signal. Drive: 2 mA at 2.4; 2 mA at 0.4 V
19	MCS/	OUT	Multiscale Enabled
			TTL Negative true signal.
20	INV/	IN	Invalid ADC Conversion
			TTL negative true signal. No function with standard 4610/4611.
21	DT	IN	Dead Time



Controls PHA Live time gating. TTL positive true signal.  $V_{in} > 2.4V$  at 0.4 mA, disables PHA Live Timer from counting.  $V_{in} < 0.5 V$ , or open circuit, enables PHA Live Timer to count.

- |    |             |   |
|----|-------------|---|
| 22 | ENDATA/OUT  | Enable Address Data   |
|    |             | TTL negative true signal. Drive: 2 mA at 2.4 V; 2 mA at 0.4 V.  |
| 23 | I/O ACK IN  | Optional; only with Model 4622. Enables I/O controls from Model 4622. TTL negative true signal.                         |
| 24 | Ground      |   |
| 25 | I/O CMD OUT | Optional; only with Model 4622. Request from Model 4622 to send control signal to Model 1520. TTL negative true signal. |

**J102 Remote Control**

8-pin female DIN Connector. Remote Control Timing is shown in Figure 52.

Unless otherwise stated, the Remote Control Signal parameters are:

Inputs: Positive = 2.4 V to 5.0 V.  
Negative = 0.0 V to 0.3 V at 1 mA.

Outputs: Positive = 2.4 to 5 V (0.4 mA at 2.4 V).  
Negative = 0.0 to 0.5 V at 2 mA.

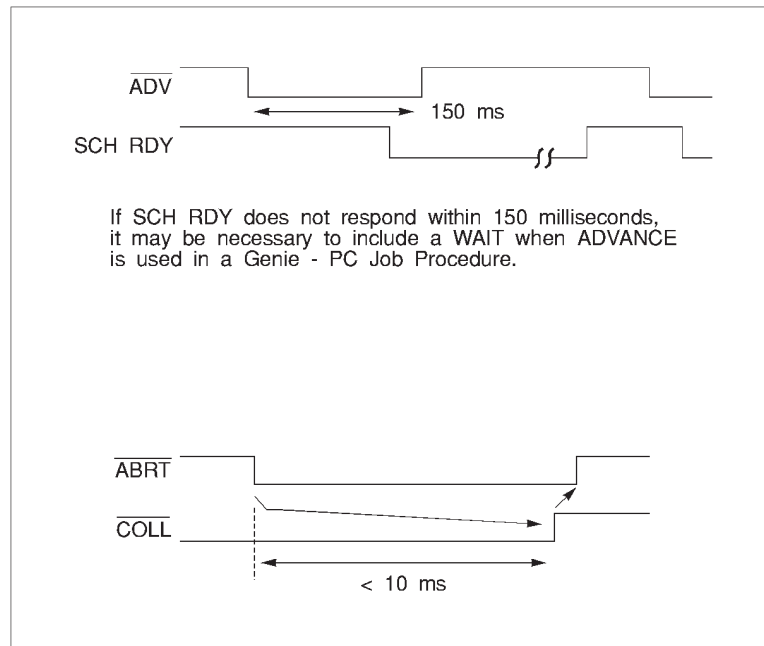


Figure 52 Remote Control Timing Diagram

<u>Pin</u>	<u>Signal</u>	<u>In/Out</u>	<u>Description</u>
1	ABRT/	IN	Abort In  TTL negative true signal. Ends Collect. Hold low until status changes (pin 4).
2	SCH RDY	IN	Sample Changer Ready In  TTL positive true signal. If SCH RDY does not respond within 150 ms, it may be necessary to include a WAIT when ADVANCE is used in a Genie-2000 Job Procedure.
3	ADV/	OUT	Advance Out  TTL negative true signal Approximate 150 ms pulse after command.
4	COLL/	OUT	Collect Status  TTL negative true signal. True (low) when in Acquire Mode.
5	Ground		
6	XRES/	IN	Reset In

TTL negative true signal. Causes hardware reset of microprocessor on MCA board. Minimum width 100 ms.

7 Ground

8 AOF IN End of Sweep In

TTL positive true signal. Used for MCS sweep counting. Minimum width 1  $\mu$ s.

### Micro Channel Host Bus Signals

Except as noted, all inputs are through CMOS (HCT) receivers for essentially zero dc loading.

A0 through A15. Address lines used for I/O device decoding. TTL positive true.

D0 through D7. Data Bus bits 0 through 7 for byte transfer IN and OUT to Host. Gated onto bus during I/O Read cycles. TTL positive true.

Bus Loading: 20.0  $\mu$ A at 2.7 V; 0.2 mA at 0.4 V.

Bus Drive: 3.0 mA at 2.4 V; 24.0 mA at 0.5 V

–ADL

Address Decode Latch. Input signal from system to latch addresses and status bits. Data valid on trailing edge of –ADL.

M/–IO

Memory/–Input Output. input signal that distinguishes a memory cycle from an I/O cycle. TTL low indicates I/O cycle in progress.

–S0,–S1

–Status bits 0 and 1. These bits are inputs that indicate the type of bus cycle.

–CMD

–Command. Input signal that defines when data on the bus is valid. The positive-going (trailing) edge of this signal indicates the end of a bus cycle.

–CD SFDBK

–Card Selected Feedback. This output signal goes active (low) when board is addressed, except during the configuration cycle. Positive: > 2.4 V at 2 mA; negative: < 0.4 V at 6 mA

**CD CHRDY**

Channel Ready. Output to signal when board requires additional time to complete a channel operation. Ready is TTL positive. Positive:  $> 2.4$  V at 2 mA; negative:  $< 0.4$  V at 6 mA

**-CD SETUP**

-Card Setup. This input is driven low during system configuration and error recovery procedures. It selects the card slot.

**CHRESET**

Channel Reset. This input is driven high to initialize the board's Micro Channel interface circuitry during power on/power fail and while doing a soft boot.

+5 V dc. Logic power to board.  $< 0.8$  A, nominal.

-12 V dc. Bias voltage to board.  $< 0.5$  mA.

## AccuSpec Boards

This section details the Rear Panel Connections and Specifications for the AccuSpec A, NaI, B, NaI Plus, and FMS boards.

For consistency, all negative true signals are followed by a slash (SIGNAL/). Note, however, that on all AccuSpec schematics negative true signals are shown by a following asterisk (SIGNAL\*).

### AccuSpec A and NaI Boards

The AccuSpec A and AccuSpec NaI boards have a BNC connector for connection to the analog input signal and a 9-pin male D-style connector which provides signals for various external applications.

A special cable is available to make the connections to the rear panel D-style connector. Standard BNC connections to the signals are provided by cable 759618. Cable 751885 is an adapter cable to allow connection to the PUR/LTC signals on the Model 2020, 2024, 2025, 2026, and 9615 amplifiers.

#### BNC Signal Input

- DC-coupled only.
- Nominally 8.0 V full scale.
- Positive monopolar or initially positive bipolar semi-Gaussian shaped pulses with a time constant of 0.5 to 10  $\mu$ s or gated integrator shaped pulses.

- Flat-top pulses with a minimum pulse width of 3.0  $\mu\text{s}$  are also acceptable
- Input impedance greater than 10  $\text{k}\Omega$

### External Signals On a 9-Pin Male D-Style

Breakout cable 759618 can be purchased separately.

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
1-5	GND	Common signal return path
6	ADT/	TTL compatible Output signal; normally +5 V.

In PHA mode, the output signal ADT/ goes low (0 - 0.5 V) when the ADC is busy processing an event. This is considered to be the ADC DEADTIME or the time during which the ADC is unable to process another input event. PHA Mode Timing is shown in Figure 53.

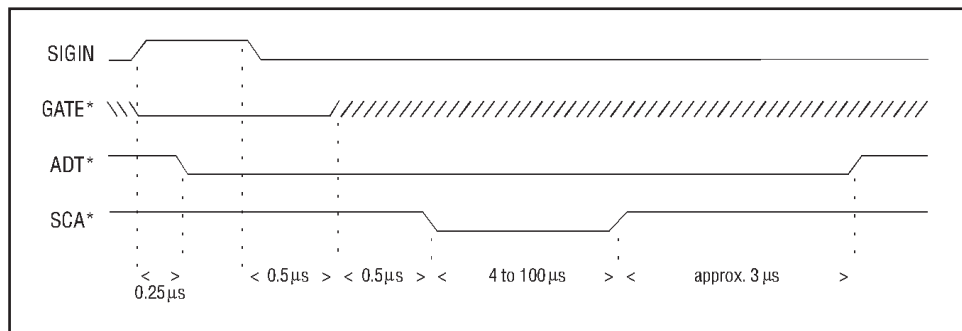


Figure 53 Timing Diagram - PHA Mode

The approximate ADC DEADTIME can be calculated according to the following formula(s):

$$100 \text{ MHz} = \text{Tr} + 4 \mu\text{s} + (\text{N} * 10 \text{ ns}) + (\text{CG}/16 * 10 \text{ ns})$$

Where:

Tr = Input pulse rise time or 1.5  $\mu$ s, whichever is greater  
 N = Channel number converted  
 CG = Conversion gain selected

In STROBE mode, the signal ADT/ goes low (0 - 0.5 V) when the input GATE/ signal is non-asserted (high) and goes high (4.5 - 5.0 V) when the GATE/ signal is asserted (low). Strobe Mode Timing is shown in Figure 54.

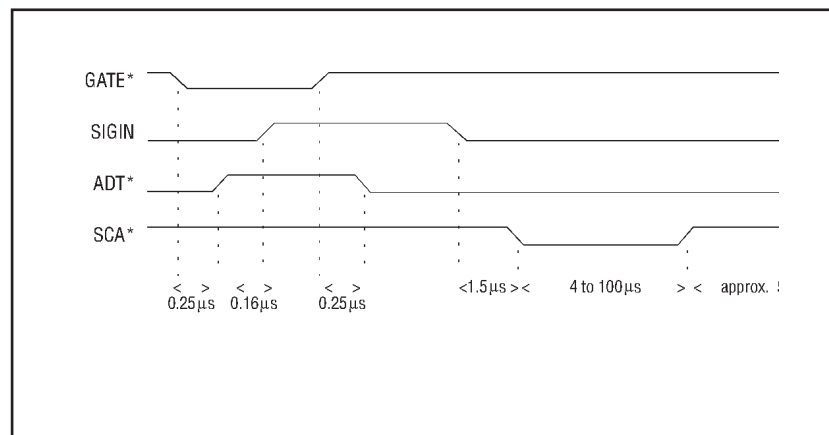


Figure 54 Timing Diagram - Strobe Mode

The ADT/ output signal can source 1 mA or sink up to 10 mA maximum. External loading of this signal in excess of these ratings should be avoided since it will interfere with the normal operation of the ADC or damage the output driver.

Alternately, signal ACQ/ may be selected as an output on pin 6. This is accomplished with a jumper option by removing jumper ADT/ and installing jumper ACQ/. ACQ/ is a TTL compatible signal that normally stays at +5 V. In either PHA or STROBE mode signal ACQ/ will go low (0 - 0.5 V) when acquisition is enabled by the CPU and returns high (4.5 - 5.0 V) when acquisition times out or is turned off by the computer system.

## 7 AMPBSY

TTL compatible input signal that allows logical ORing of an amplifier busy signal with the internal ADC busy signal.

The AMPBSY input signal allows control of the MCA live time clock from an external signal. This signal will stop the MCA live time clock when asserted (4.5 - 5.0 V). The MCA live time clock will be allowed to run only when:

Acquisition is enabled, AMPBSY signal is not asserted (0 - 0.5 V) and the ADC is not busy (signal ADT/ is high).

The AMPBSY input signal impedance is 1 k $\Omega$ .

TTL high: +3.5 to 5.0 V

TTL low: 0.0 to 0.5 V

Alternately, the polarity of the AMPBSY input signal may be inverted. This can be accomplished with a jumper option by removing jumper BUSY and installing jumper BUSY/. This jumper allows a low signal to stop the MCA live time clock.

When used with the Model 2020, 2024, 2025, 2026 or 9615 Amplifiers in PUR/LTC mode, the jumper must be in the BUSY/ position.

8

SCA/

TTL compatible output signal that provides a negative going output pulse for every event that falls within the LLD/ULD window.

The SCA/ output signal is normally high (4.5 - 5.0 V) and goes low (0 - 0.5 V) whenever the ADC has converted an event. Since no event is converted unless its amplitude falls between the LLD and ULD (lower and upper level discriminators), this signal can be used as the output of SCA (single channel analyzer). The duration of the SCA/ signal is a function of the ADC conversion time.

During normal PHA mode acquisition, the length of this pulse represents the conversion time of the ADC. In SCA mode, this pulse is typically 1 to 2  $\mu$ s, maximum. External loading of this signal in excess of these ratings should be avoided since it will interfere with the normal operation of the ADC or damage the output driver.

Alternately, signal LG/ may be selected as an output on pin 8. This is accomplished with a jumper option by removing jumper SCA/ and installing jumper LG/.

Signal LG/ is used for live time correction with the Model 2020, 2024, 2025, 2026 or 9615 Amplifiers in PUR/LTC mode.

Signal LG/ goes low (0 - 0.5 V) when an input pulse crosses the lower level discriminator (LLD) and remains low until the peak of the input pulse.

9

#### GATE/

TTL compatible input signal used to control the linear gate. (+5 V disables linear gate.) This signal may be used for PUR, coincidence gating, or trigger in STROBE mode.

With the Model 2020, 2024, 2025, 2026 or 9615 Amplifiers, the jumper is in the GATE/ position for PUR/LTC mode.

In PHA mode, the GATE/ signal may be used to selectively reject events converted by the ADC. As an example, it may be connected to the INHIBIT or BLOCK output of a nuclear spectroscopy amplifier to reject events subject to pulse pileup.

A low (0 - 0.5 volt) GATE/ signal is normal and this allows all incoming events to be converted and stored. A high (4.5 - 5.0 volt) GATE/ signal inhibits all incoming events from being converted and stored. In order for the ADC to convert and store an event, the GATE/ signal must be low BEFORE the input pulse arrives at the ADC and must remain low a minimum of 0.5  $\mu$ s after the peak amplitude of the input pulse.

Allowing the GATE/ signal to go high any time during the rise time of the input pulse will cause the event to be rejected (the ADC will be reset and no count added to memory).

With the Model 2020, 2024, 2025, 2026 or 9615 Amplifiers, the jumper is in the GATE/ position for PUR/LTC mode.

In STROBE mode, the GATE/ signal serves as an external trigger to start the ADC conversion. Normally, a negative going pulse should be used to start the operation. When the GATE/ signal goes from the high to the low state, the ADC linear gate will open and sample the voltage applied to the input. The linear gate will remain open as long as the GATE/ signal remains in the low state. Approximately 1.5  $\mu$ s after the GATE/ signal switches back to the high state, the linear gate will close and the conversion will commence. The duration of the GATE/ signal must be a minimum of 1  $\mu$ s in either the high or low state.

The minimum time that the linear gate can be open is about 2.5  $\mu$ s.

STROBE mode is selected by removing jumper PHA and installing jumper STB.



The GATE/ input signal impedance is 1 k $\Omega$ .

A logical 0 = 4.5 - 5.0 V. A logical 1 = 0.0 - 0.5 V

Alternately, the polarity of the GATE/ input signal may be inverted. This can be accomplished with a jumper option by removing jumper GATE/. This jumper option allows a low signal (0 - 0.5 V) to inhibit incoming events in PHA mode or allows the use of a positive GATE pulse in STROBE mode.

When any of the AMX modules (Models 589 or 8224) is to be used, the STROBE mode must be enabled and the Gate polarity is negative true (GATE/).

## AccuSpec B Board

The AccuSpec B board have the ADC interface on a 37-pin male D-style connector. An external MCA to ADC interface cable is provided with the board.

<u>Pin</u>	<u>Wire</u>	<u>Signal</u>	<u>Description</u>
1-6	1,3,5 7,9,11	GND	Logic signal common
7	13	ADC13/	Input data lines ADC0/ through ADC13/ are TTL compatible devices. Logic 1 = 0 to 0.5 V, Logic 0 = 2.5 to 5.0 V. $Z_{in} = 2.2 \text{ k}\Omega$ to +5 V. Data will be latched on the leading edge of the CLADC pulse.
8	15	ADC7/	
9	17	ADC8/	
10	19	ADC9/	
11	21	ADC10/	
12	23	ADC11/	
13	25	ADC12/	
14	27	Reserved	
15	29	Reserved	
16	31	Reserved	
17	33	Reserved	
18	35	Reserved	
19	37	Reserved	
20	2	CLADC/	Clear ADC output

The steady state condition of signal CLADC/ is +5 V. The ADC interface logic resets when signal CLADC/ goes from +5 to 0 V. A pulse duration of 1  $\mu$ s is provided. Logic 1 = 0 V at 10 mA Logic 0 = 2.5 - 5.0 V at 1 mA

21	4	ATR/	ADC transfer output
			The steady state condition of signal ATR/ is +5 V. Data transfer occurs when signal ATR/ goes from +5 V to 0 V. A pulse duration of 1 $\mu$ s is provided. Logic 1 = 0 V at 10 mA Logic 0 = 2.5 to 5.0 V at -1 mA
22	6	ADCB/	ADC busy input (live time)
			ADCB/ represents the time the ADC cannot validly accept input pulses; that is, the linear gate is closed. When not in acquire mode, ADCB/ should remain at +5 V. (ADCB/ is intended to be used for live time control.) Input impedance = 2.2 k $\Omega$ to +5 V
23	8	ACQ/	Acquire output
			Signal ACQ/ switches to 0 V to enable the ADC or +5 V to disable the ADC.
24	10	READY/	Ready Input
			The steady state condition of signal READY/ is +5 V. When ADC conversion is complete, signal READY is pulled low, signaling the computer that data is ready to be transferred. Input impedance = 2.2 k $\Omega$ to +5 V
25	12	INH/	Inhibit Input
			Signal INH/ is at +5 V when information is acceptable and at 0 V when information is to be rejected. Input impedance = 2.2 k $\Omega$ to +5 V.
26	14	ADC0/	Input data lines ADC0/ through ADC13/ are TTL compatible devices.
27	16	ADC1/	
28	18	ADC2/	
29	20	ADC3/	
30	22	ADC4/	
31	24	ADC5/	
32	26	ADC6/	
33	28	Reserved	
34	30	Reserved	
35	32	Reserved	

36	34	Reserved
37	36	Reserved

## AccuSpec/NaI Plus Board

The AccuSpec NaI/Plus board has a BNC connector for amplifier input, a SHV connector for high voltage output, and a 9-pin female D-style connector for preamp power output.

### BNC Amplifier Signal Input

- Voltage Sensitive input accepts positive or negative tail pulses.
- 0 to 12 V maximum
- Rise time <math><0.5 \mu\text{s}</math>
- Decay time constant = 40  $\mu\text{s}$  to  $\infty$  (factory set to 50  $\mu\text{s}$ ).
- Input impedance  $\approx 470 \Omega$

### SHV High Voltage Output

- 0 to +1.0 kV at 300  $\mu\text{A}$

Preamp Power on a 9-Pin Female D-Style Connector

Six inch C1552 Adapter Cable is provided with the board.

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
1-2	GND	Common power return path
3	KEY	Key position
4	+12 V	+12 V preamp power
5	KEY	Key position
6-7	N/C	No connection
8	KEY	Keyed position
9	-12V	-12 V preamp power

## AccuSpec FMS Board

The AccuSpec FMS is a full-sized PC/XT card which can work concurrently with the AccuSpec family of MCA boards in multi-board configurations. The FMS board has a BNC connector for the SCA analog input and a 15-pin DB connector for TTL input and output control signals.

### BNC Signal Input

This BNC connects to the input of the SCA. An analog signal, in the form of positive pulses, is applied through this BNC connector. The voltage range is 0 to 8 V with an input impedance 1 K $\Omega$ . Maximum counting frequency is 1 MHz.

### External Signal On a 15-Pin DB Connector

All the input control and output status signals are provided through this connector. The TTL input signal, allowing count rates to 100 MHz, is provided here also.

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
1	DAC	Analog output signal (0 to +5 V). This amplitude of this signal is proportional to the current sweep channel address, 5 volts representing the last channel and 0 volts representing the first channel.
2	SCA*	TTL output signal. This signal is the negative pulse from the SCA.
3	E0CH*	TTL output signal. A positive pulse, of which the transition from high to low indicates the end of the channel dwell time.
4	TRIG*	TTL input signal. A transition from low to high starts an MCS sweep. The signal can then be brought low during the sweep. A continuous high level allows continuous sweeps until the preset is reached.
5	ADV*	TTL input signal. A transition from low to high (negative pulse recommended) terminates the current dwell time and advances the channel address.
7	“TTL”	TTL input signal. A positive pulse applied to this signal causes one count to be added to memory at the current channel address. The count occurs on the low to high transition. The pulse width must be a minimum of 5 ns for rates up to 100 MHz. Input impedance is 50 $\Omega$ . Input low = 0 to 0.5 V. Input high = 2.5 to 5 V. This input signal is not protected against over voltage. Under <i>no circumstances</i> should the input signal level be greater than 5.5 V or less than -0.5 V.
12	ACQEN*	TTL output signal. This signal indicates that acquisition is in progress. ACQEN* goes low at the start and high at the end of a sweep provided XTRIG is being used. In continuous sweep mode, XTRIG goes low at the start of the first sweep and high at the end of the last sweep.
13	EOP	TTL output signal. This signal switches high at mid sweep and low at sweep end.

## AccuSpec A and NaI Specifications

The AccuSpec A and AccuSpec NaI boards are plug-In MCA boards for an IBM PC or compatible PCs. The AccuSpec A board contains a computer-controlled, 8K channel, 100 MHz on-board Wilkinson-type ADC plus 8K channels of spectral memory. The AccuSpec NaI board contains a computer-controlled, 2K channel, 100 MHz on-board Wilkinson-type ADC plus 2K channels of spectral memory.

Conversion Gain (channels full scale, software selectable) - 256, 512, 1024, 2048, 4096 or 8192 (A); 256, 512, 1024 or 2048 (NaI).

Clock Rate (All Conversion Ranges) - 100 MHz

Signal Input - Amplitude: 0 to +8 V, nominal; dc coupled; Input Impedance = 10 k $\Omega$

Polarity - Positive monopolar or initially positive bipolar semi-Gaussian or gated integrator shaped pulses with shaping times from 0.5 to 10  $\mu$ s or flat top pulses with a minimum width of 3  $\mu$ s.

Integral Linearity -  $> \pm 0.05\%$  over the top 99% of full scale.

Differential Linearity -  $< 1.0\%$  deviation from mean channel width over the top 99% full scale.

Temperature Stability -  $< \pm 0.01\%$  gain shift and less than  $\pm 0.005\%$  zero drift per 1  $^{\circ}$ C from 0 to 50  $^{\circ}$ C.

ULD/LLD - Adjustable from 0 to 100% of full scale via software control.

Fine LLD - Adjustable from 0 to 6% of full scale via software control.

Analog Zero - Adjustable between  $\pm 3\%$  of full scale via software control.

PHA Mode - Pulse height analysis with or without coincidence gating.

SCA Mode - The ADC can be operated as a gated or ungated single channel analyzer.

Strobe Mode - The ADC can be operated in a sample voltage analysis mode using an external strobe at rates up to 70 kHz, conversion gain dependent.

Rear Panel Connector - SIGNAL BNC: 9-pin D-type connector for GATE, AMP BUSY, SCA and DT signals.

Rear Panel Indicator - BUSY LED.

Dimensions - 32.8 x 9.9 cm (12.9 x 3.9 in.).

Weight - Approximately 0.45 kg (1 lb).

Operating Temperature Range - 0 to 50 °C.

Power Requirements - +5 V dc at 1.6 A, max.

## **AccuSpec B Specifications**

The AccuSpec B Board is a plug-in MCA board for the IBM PC or compatible computer. The AccuSpec B contains 16K data channels of spectral memory. C1704 Interface Cable included for connection to ADCs with 34-pin ribbon connector.

Dimensions - 32.8 x 9.9 cm (12.9 x 3.9 in.).

Weight - Approximately 0.45 kg (1 lb).

Operating Temperature Range - 0 to 50 °C.

Power Requirements - +5 V dc at 0.8 A, max.

## **AccuSpec/NaI Plus Specifications**

The AccuSpec/NaI Plus board is a plug-in MCA board for IBM PCs or compatible computers. This board contains complete front end electronics for connection to photomultiplier type (PMT) preamp base assemblies, allowing PHA acquisition from NaI or other scintillation detectors.

### **Wilkinson ADC**

Conversion Gain (Channels Full Scale, software Selectable) - 256, 512, 1024, 2048.

Clock Rate (All Conversion Ranges) - 100 MHz.

Integral Nonlinearity - Less than  $\pm 0.02\%$  of full scale over the top 99% of selected range.

Differential Nonlinearity - Less than 1.0% deviation from mean channel width over the top 99% full scale.

Gain Drift -  $< 0.01\%/^{\circ}\text{C}$ .

Zero Drift -  $< 0.005\%$  of full scale per  $^{\circ}\text{C}$ .

ULD/LLD - Adjustable from 0 to 100% of full scale via software control.

Fine LLD - Adjustable from 0 to 6% of full scale via software control.

Analog Zero - Adjustable between  $\pm 3\%$  of full scale via software control.

Mode - Pulse Height Analysis (PHA).

### **Amplifier**

Input Signal - Voltage sensitive input accepts positive or negative tail pulses from an associated preamplifier; amplitude 0 to  $\pm 12$  V, maximum; polarity positive or negative, software selectable; rise time  $< 0.5$   $\mu$ s; decay time constant 40  $\mu$ s to  $\infty$  (factory set to 50  $\mu$ s) internal pole/zero adjustment; input impedance 470  $\Omega$ ; board mounted rear panel BNC connector.

Gain - Programmable from X2 to X1000.

Pulse Shape - Bipolar 1  $\mu$ s shaping time constant; time to peak 1.3  $\mu$ s; time to cross-over 2.5  $\mu$ s; pulse width 10  $\mu$ s.

Integral Nonlinearity -  $< \pm 0.1\%$  of full scale output measured at gain of 150.

Peak Shift -  $< \pm 0.05\%$  of full scale to 25 kHz.

Gain Drift -  $< 0.02\%/^{\circ}\text{C}$ .

Zero Drift -  $< 25$  mV/ $^{\circ}\text{C}$ .

Noise Contribution -  $< 35$  mV rms referenced to input at maximum gain.

Overload Recovery - Recovers to within  $\pm 2\%$  of full scale output from X200 overload in 20  $\mu$ s when properly pole/zeroed.

### **High Voltage Power Supply:**

Power - 0 to 1.0 kV at 300  $\mu$ A, continuously adjustable via software control.

Control - Software control of on/off and HV setting.

Resolution - HV settable within 0.4% of full scale.

Nonlinearity -  $< \pm 0.3\%$  of full scale.

Calibration Error -  $<\pm 0.2\%$  of full scale.

Drift -  $<\pm 0.01\%/^{\circ}\text{C}$  after 30 minute warmup.

Regulation - Line  $<\pm 0.05\%$  from 10% change in supply voltage; load  $<\pm 0.3\%$  at 0 to 300  $\mu\text{A}$ .

Output Ripple -  $<20$  mV peak-peak at full load, dc to 1 MHz.

Overload Protection - Short circuit proof; must be reset by software to turn on after fault removed.

HV Indicator - Board mounted rear panel LED indicates HV on.

Dimensions - 30.5 x 9.9 x 2.0 cm (12 x 3.9 x 0.8 in.)

Weight - 0.68 kg (1.5 lb)

Operating Temperature Range - 0 to 35  $^{\circ}\text{C}$ , ambient

Power Requirements - +5V dc at 1.5 A, +12 V dc at 150 mA, -12 V dc at 100 mA.  
(Includes loading contributed by 2007P Tube-base Preamp at maximum HV setting.)

## Outputs

HV Output - 0 to +1.0 kV at 300  $\mu\text{A}$ , adjustable via software control; board rear panel mounted SHV connector.

Preamp Power -  $\pm 12\text{V}$  for powering external preamplifier; board rear panel mounted 9-pin female D-style connector; C1552 Adapter Cable provided with board.

## AccuSpec FMS Board Specifications

The AccuSpec FMS provides multi-channel scaling capability to any PC system equipped with a spare ISA connector capable of accepting a standard full size board. The FMS board includes 64K byte SRAM for on-board data storage of up to 16K channels. In addition, the board contains a SCA for counting output pulses directly from a detector/amplifier front-end and an optional DAC for applications requiring an analog ramp output.

Input Count Rate - 100 MHz for TTL signal, 1 MHz for SCA input

Dwell Time - Adjustable from 2  $\mu\text{s}$  to 1 hr via software control.



## Technical Information

Interchannel Dead Time - < 10 ns

Intersweep - < 10 ns

Sweep Counter - 1 to 65 536

Counts per Channel -  $2^{31} - 1$

SCA LLD/ULD - Adjustable from 0 to 100% of full scale via software control.

Dimensions - 32.77 x 9.91 cm (12.9 x 3.9 in.)

Weight - 0.45 kg (1.0 lb)

Operating Temperature Range - 0 to 50 °C.

Power Requirements - +5 V dc at 1.6 A, max.

## Troubleshooting

If Canberra Customer Service assistance is needed, please note the Genie-2000 software version number, and for the System 100, the MCA board's firmware version number. The software version number is shown on the label of the Genie-2000 Installation CD. The MCA board's Firmware Version can be found on the labels attached to:

Chips A25 and A26 on S100 ISA Bus MCAs (Figure 55).

Chip A18 on S100 Micro Channel Bus MCAs (Figure 56)

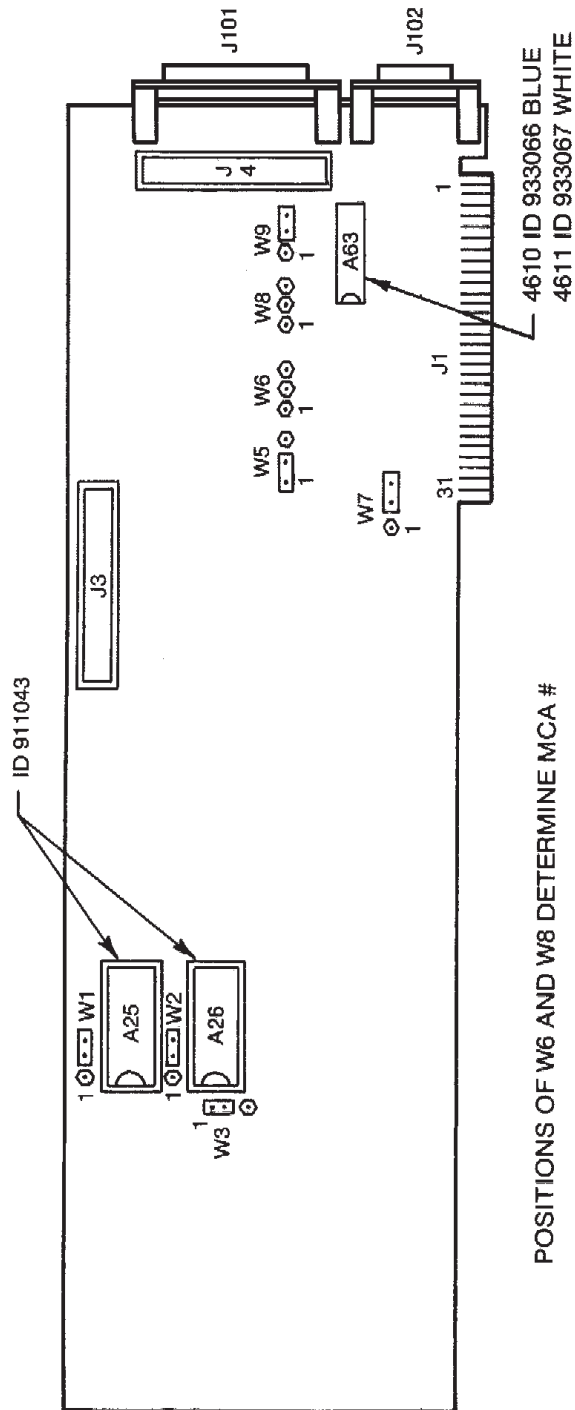


Figure 55 System 100 IPC Board Layout

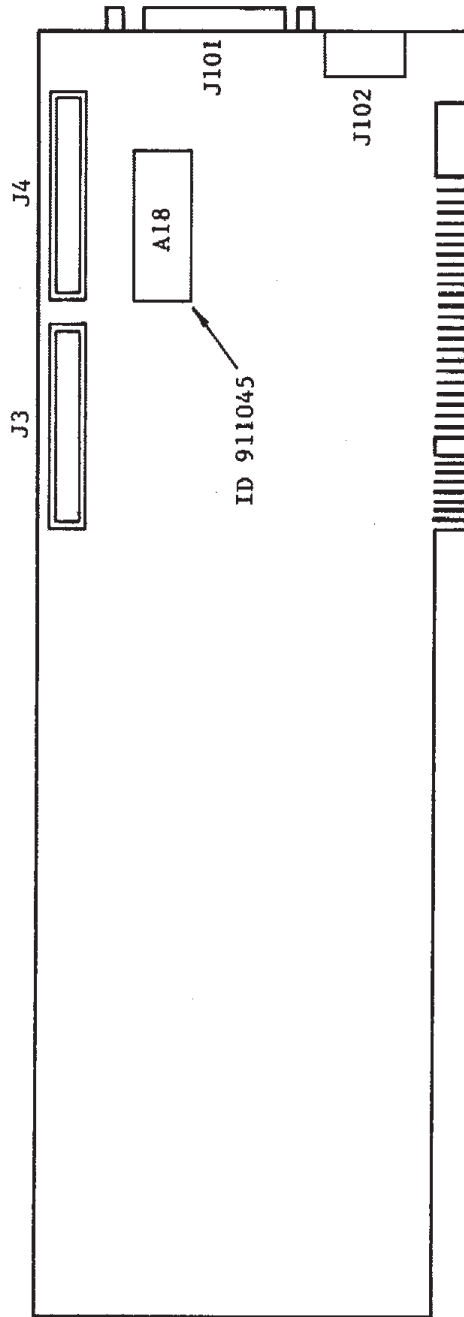


Figure 56 System 100 Micro Channel Board Layout

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## Warranty

Canberra's product warranty covers hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

### DOMESTIC WARRANTY

Canberra (we, us, our) warrants to the customer (you, your) that equipment manufactured by us shall be free from defects in materials and workmanship under normal use for a period of one (1) year from the date of shipment.

We warrant proper operation of our software only when used with software and hardware supplied by us and warrant that our software media shall be free from defects for a period of 90 days from the date of shipment.

If defects are discovered within 90 days of receipt of an order, we will pay for shipping costs incurred in connection with the return of the equipment. If defects are discovered after the first 90 days, all shipping, insurance and other costs shall be borne by you.

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We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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